SIEMENS

SIMATIC

S7-300
CPU 31xC and CPU 31x, Technical Data

Manual

The following supplement is part of this documentation:

No.	Designation	Drawing number	Edition
1	Product information	A5E00688649-02	03/2006

This manual is included in the documentation package with Order No.: 6ES7398-8FA10-8BA0

01/2006 Edition
A5E00105475-06

Safety Guidelines

This manual contains notices you have to observe in order to ensure your personal safety, as well as to prevent damage to property. The notices referring to your personal safety are highlighted in the manual by a safety alert symbol, notices referring only to property damage have no safety alert symbol. These notices shown below are graded according to the degree of danger.

Danger

indicates that death or severe personal injury **will** result if proper precautions are not taken.

Warning

indicates that death or severe personal injury **may** result if proper precautions are not taken.

Caution

with a safety alert symbol, indicates that minor personal injury can result if proper precautions are not taken.

Caution

without a safety alert symbol, indicates that property damage can result if proper precautions are not taken.

Notice

indicates that an unintended result or situation can occur if the corresponding information is not taken into account.

If more than one degree of danger is present, the warning notice representing the highest degree of danger will be used. A notice warning of injury to persons with a safety alert symbol may also include a warning relating to property damage.

Qualified Personnel

The device/system may only be set up and used in conjunction with this documentation. Commissioning and operation of a device/system may only be performed by **qualified personnel**. Within the context of the safety notes in this documentation qualified persons are defined as persons who are authorized to commission, ground and label devices, systems and circuits in accordance with established safety practices and standards.

Prescribed Usage

Note the following:

Warning

This device may only be used for the applications described in the catalog or the technical description and only in connection with devices or components from other manufacturers which have been approved or recommended by Siemens. Correct, reliable operation of the product requires proper transport, storage, positioning and assembly as well as careful operation and maintenance.

Trademarks

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Disclaimer of Liability

We have reviewed the contents of this publication to ensure consistency with the hardware and software described. Since variance cannot be precluded entirely, we cannot guarantee full consistency. However, the information in this publication is reviewed regularly and any necessary corrections are included in subsequent editions.

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Order No.: A5E00105475-06
Edition 0102/2006

Preface

Purpose of the Manual

This manual contains all the information you will need concerning the configuration, communication, memory concept, cycle, response times and technical data for the CPUs. You will then learn the points to consider when upgrading to one of the CPUs discussed in this manual.

Required basic knowledge

- To understand this manual, you require a general knowledge of automation engineering.
- You should also be accustomed to working with STEP 7 basic software.

Area of application

Table 1 Application area covered by this manual

CPU	Convention: CPU designations:	Order number	as of version	
			Firmware	Hardware
CPU 312C	CPU 31xC	6ES7312-5BD01-0AB0	V2.0.0	01
CPU 313C		6ES7313-5BE01-0AB0	V2.0.0	01
CPU 313C-2 PtP		6ES7313-6BE01-0AB0	V2.0.0	01
CPU 313C-2 DP		6ES7313-6CE01-0AB0	V2.0.0	01
CPU 314C-2 PtP		6ES7314-6BF02-0AB0	V2.0.0	01
CPU 314C-2 DP		6ES7314-6CF02-0AB0	V2.0.0	01
CPU 312	CPU 31x	6ES7312-1AD10-0AB0	V2.0.0	01
CPU 314		6ES7314-1AF11-0AB0	V2.0.0	01
CPU 315-2 DP		6ES7315-2AG10-0AB0	V2.0.0	01
CPU 315-2 PN/DP		6ES7315-2EG10-0AB0	V2.3.0	01
CPU 317-2 DP		6ES7317-2AJ10-0AB0	V2.1.0	01
CPU 317-2 PN/DP		6ES7317-2EJ10-0AB0	V2.3.0	01
CPU 319-3 PN/DP		6ES7318-3EL00-0AB0	V2.4.0	01

Note

For information on the special features of the CPU 315F-2 DP (6ES7 315-6FF00-0AB0) and CPU 317F-2 DP
(6ES7 317-6FF00-0AB0), refer to the product information in the Internet:
http://support.automation.siemens.com under article ID 17015818.

Note

There you can obtain the descriptions of all current modules. For new modules, or modules of a more recent version, we reserve the right to include a Product Information containing latest information.

Changes in comparison to the previous version

Compared to the previous version of this manual CPU31xC and CPU31x, Technical Data, with the footnote number: A5E00105475-05, Release 08/2004, there are following changes:

- CPU 319-3 PN/DP, 6ES7 318-3EL00-0AB0, Firmware V2.4.0, supplemented
- Product information A5E00385496-01 integrated into manual

New features of CPU 319-3 PN/DP:

- Increased instruction-processing performance
- Expansion of quantity structures:
  - 1.4 MB work memory
  - 4096 modules
- CPU with 3 interfaces (1xMPI/DP, 1xDP and 1xPN)
- Isochronous mode for a sub-process diagram
- New system functions:
  - Measuring initiator for diagnostic repeater (SFC 103)
- New message blocks (SFC105-108)
- Addition of following protocol versions to open communication via Industrial Ethernet:
  - Connection oriented protocol: ISO on TCP according to RFC 1006
  - Connectionless protocol: UDP according to RFC 768

Approvals

The SIMATIC S7-300 product series has the following approvals:

- Underwriters Laboratories, Inc.: UL 508 (Industrial Control Equipment)
- Canadian Standards Association: CSA C22.2 No. 142, (Process Control Equipment)
- Factory Mutual Research: Approval Standard Class Number 3611

CE label

The SIMATIC S7-300 product series satisfies the requirements and safety specifications of the following
EC Directives:

- EC Directive 73/23/EEC "Low-voltage directive"
- EC Directive 89/336/EEC "EMC directive"

C tick mark

The SIMATIC S7-300 product series is compliant with AS/NZS 2064 (Australia).

Standards

The SIMATIC S7-300 product series is compliant with IEC 61131-2.

Documentation classification

This manual is part of the S7-300 documentation package.

Name of the manual	Description
YOU ARE READING the Manual • CPU 31xC and CPU 31x, Technical Specifications	Operation and display elements, communication, memory concept, cycle and response times, technical specifications
Operating Instructions • S7-300, CPU 31xC and CPU 31x: Installation	Configuration, installation, wiring, addressing, commissioning, maintenance and the test functions, diagnostics and troubleshooting.
System Manual PROFINET System Description	Basic information on PROFINET: Network components, data exchange and communication, PROFINET IO, Component Based Automation, sample application PROFINET IO and Component Based Automation
Programming Manual From PROFIBUS DP to PROFINET IO	Guideline for the migration from PROFIBUS DP to PROFINET I/O.
Manual • CPU 31xC: Technological functions • Examples	Description of the individual technological functions Positioning, Counting. PtP communication, rules The CD contains examples of the technological functions
Reference Manual • S7-300 Automation System: Module data	Descriptions of functions and technical specifications of signal modules, power supply modules and interface modules
Instruction List • CPU 31xC and CPU 31x	List of operation repertoire of CPU and its execution times. List of executable blocks.

Name of the manual	Description
Getting Started The following Getting Started editions are available as a collective volume: • CPU 31x: Commissioning • CPU 31xC: Commissioning • CPU 31xC: Positioning with analog output • CPU 31xC: Positioning with digital output • CPU 31xC: Counting • CPU 31xC: Rules • CPU 31xC: PtP communication • CPU 315-2 PN/DP, 317-2 PN/DP, CPU 319-3 PN/DP: Configuring the PROFINET interface • CPU 317-2 PN/DP: Configuring an ET 200S as PROFINET IO device • CPU 443-1 Advanced: Configuration of the PROFINET interface with an IE/PB-Link and ET 200B	The example used in this Getting Started guides you through the various steps in commissioning required to obtain a fully functional application.

Additional information required:

Name of the manual	Description
Reference Manual System software for S7-300/400 system and standard functions	Description of the SFCs, SFBs and OBs. This manual is part of the STEP 7 documentation package. For further information, refer to the STEP 7 Online Help.
Manual SIMATIC NET: Twisted Pair and Fiber-Optic Networks	Description of Industrial Ethernet networks, network configuration, components, installation guidelines for networked automation systems in buildings, etc.
Manual Component Based Automation: Configure SIMATIC iMap plants	Description of the SIMATIC iMap configuration software
Manual Component Based Automation: SIMATIC iMap STEP 7 AddOn, create PROFINET components	Descriptions and instructions for creating PROFINET components with STEP 7 and for using SIMATIC devices in Component Based Automation
Manual Isochronous mode	Description of the system property "Isochronous mode"
Manual Programming with STEP 7 V5.3	Programming with STEP 7
Manual SIMATIC communication	Basics, services, networks, communication functions, connecting PGs/OPs, engineering and configuring in STEP 7.

Recycling and Disposal

The devices described in this manual can be recycled, due to their ecologically compatible components. For environment-friendly recycling and disposal of your old equipment, contact a certified disposal facility for electronic scrap.

Table of contents

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Guide to the S7-300 documentation

1

Overview

There you find a guide leading you through the S7-300 documentation.

Selecting and configuring

Table 1-1 Ambient influence on the automation system (AS)

Information on..	is available in ...
What provisions do I have to make for AS installation space?	S7-300, CPU 31xC and CPU 31x operating instructions: Installation: Configuring - Component dimensions S7-300, CPU 31xC and CPU 31x operating instructions: Installation: Mounting - Installing the mounting rail
How do environmental conditions influence the AS?	S7-300, CPU 31xC and CPU 31x operating instructions: Installation: Appendix

Table 1-2 Galvanic isolation

Information on..	is available in ...
Which modules can I use if electrical isolation is required between sensors/actuators?	S7-300, CPU 31xC and CPU 31x operating instructions: Hardware and Installation: Configuring – Electrical assembly, protective measures and grounding Module Data Manual
Under what conditions do I have to isolate the modules electrically? How do I wire that?	S7-300, CPU 31xC and CPU 31x operating instructions: Hardware and Installation: Configuring – Electrical assembly, protective measures and grounding CPU 31xC and CPU 31x operating instructions: Installation: Wiring
Under which conditions do I have to isolate stations electrically? How do I wire that?	S7-300, CPU 31xC and CPU 31x operating instructions: Installation – Configuring – Configuring subnets

Table 1-3 Communication between sensors/actuators and the PLC

Information on..	is available in ...
Which module is suitable for my sensor/actuator?	For CPU: CPU 31xC and CPU 31x Manual, Technical Data For signal modules: Reference manual of your signal module
How many sensors/actuators can I connect to the module?	For CPU: CPU 31xC and CPU 31x Manual, technical data of signal modules: Reference manual of your signal module
To connect my sensors/actuators to the PLC, how do I wire the front connector ?	S7-300, CPU 31xC and CPU 31x operating instructions: Installation: Wiring – Wiring the front connector
When do I need expansion modules (EM) and how do I connect them?	S7-300, CPU 31xC and CPU 31x operating instructions: Hardware and Installation: Configuring – Distribution of modules to several racks
How to mount modules on racks / mounting rails	S7-300, CPU 31xC and CPU 31x operating instructions: Installation: Assembly – Installing modules on the mounting rail

Table 1-4 The use of local and distributed I/O

Information on..	is available in ...
Which range of modules do I want to use?	For local I/O and expansion devices: Module Data reference manual For distributed I/O and PROFIBUS DP: Manual of the relevant I/O device

Table 1-5 Configuration consisting of the Central Unit (CU) and Expansion Modules (EMs)

Information on..	is available in ...
Which rack / mounting rail is most suitable for my application?	S7-300, CPU 31xC and CPU 31x operating instructions: Hardware and Installation: Configuration
Which interface modules (IM) do I need to connect the EMs to the CU?	S7-300, CPU 31xC and CPU 31x operating instructions: Hardware and Installation: Configuring – Distribution of modules to several racks
What is the right power supply (PS) for my application?	S7-300, CPU 31xC and CPU 31x operating instructions: Hardware and Installation: Configuration

Table 1-6 CPU performance

Information on..	is available in ...
Which memory concept is best suited to my application?	CPU 31xC and CPU 31x Manual, Technical Data
How do I insert and remove Micro Memory Cards?	S7-300, CPU 31xC and CPU 31x operating instructions: Installation: Commissioning – Commissioning modules – Removing / inserting a Micro Memory Card (MMC)
Which CPU meets my demands on performance?	S7-300 instruction list: CPU 31xC and CPU 31x
Length of the CPU response / execution times	CPU 31xC and CPU 31x Manual, Technical Data
Which technological functions are implemented?	Technological Functions Manual
How can I use these technological functions?	Technological Functions Manual

Table 1-7 Communication

Information on..	is available in ...
Which principles do I have to take into account?	Communication with SIMATIC Manual PROFINET System Manual, System Description
Options and resources of the CPU	CPU 31xC and CPU 31x Manual, Technical Data
How to use communication processors (CPs) to optimize communication	CP Manual
Which type of communication network is best suited to my application?	S7-300, CPU 31xC and CPU 31x operating instructions: Hardware and Installation: Configuring – Configuring subnets
How to network the various components	S7-300, CPU 31xC and CPU 31x operating instructions: Hardware and Installation: Configuring – Configuring subnets
What to take into account when configuring PROFINET networks	SIMATIC NET Manual, Twisted-Pair and Fiber Optic Networks (6GK1970-1BA10-0AA0) – Network Configuration PROFINET System Manual, System Description – Installation and Commissioning

Table 1-8 Software

Information on..	is available in ...
Software requirements of my S7-300 system	CPU 31xC and CPU 31x Manual, Technical Data – Technical Data

Table 1-9 Supplementary features

Information on..	is available in ...
How to implement monitor and modify functions (Human Machine Interface)	For text-based displays: The relevant Manual For Operator Panels: The relevant Manual For WinCC: The relevant Manual
How to integrate process control modules	For PCS7: The relevant Manual
What options are offered by redundant and fail-safe systems?	S7-400H Manual – Redundant Systems Fail-Safe Systems Manual
Information to be observed when migrating from PROFIBUS DP to PROFINET IO	Programming Manual: From PROFIBUS DP to PROFINET IO

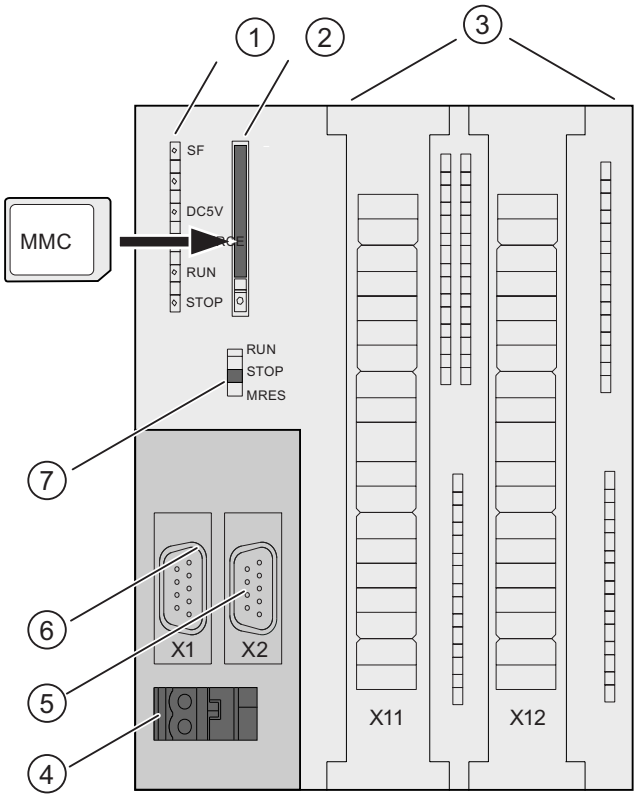
Operating and display elements

2

2.1 Operating and display elements: CPU 31xC

2.1.1 Operating and display elements: CPU 31xC

Operating and display elements of CPU 31xC



The figures show	the following CPU elements
(1)	Status and error displays
(2)	Slot for the SIMATIC Micro Memory Card (MMC) incl. the ejector
(3)	Connections of the integrated I/O.
(4)	Power supply connection
(5)	2. Interface X2 (PtP or DP)
(6)	1. Interface X1 (MPI)
(7)	Mode selector switch

The figure below illustrates the integrated digital and analog I/Os of the CPU with open front covers.

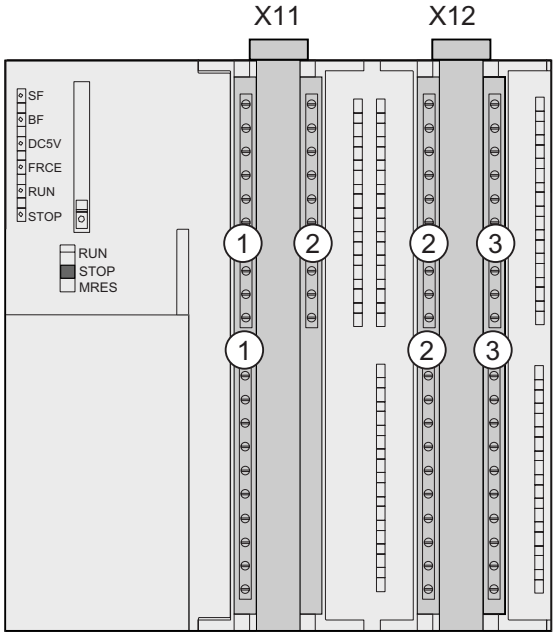


Figure 2-1 Integrated I/Os of CPU 31xC (CPU 314C-2 PtP, for example)

The figures show	the following integrated I/Os
(1)	Analog I/Os
(2)	each with 8 digital inputs
(3)	each with 8 digital outputs

Slot for the SIMATIC Micro Memory Card (MMC)

Memory module is a SIMATIC Micro Memory Card. You can use MMCs as load memory and as portable storage medium.

Note

These CPUs do not have an integrated load memory and thus require an SIMATIC Micro Memory Card for operation.

Mode selector switch

Use the mode selector switch to set the CPU operating mode.

Table 2-1 Mode selector switch settings

Position	Meaning	Description
RUN	RUN mode	The CPU executes the user program.
STOP	STOP mode	The CPU does not execute a user program.
MRES	CPU memory reset	Mode selector switch position with pushbutton function for CPU memory reset. A CPU memory reset by means of mode selector switch requires a specific sequence of operation.

Reference

- CPU operating modes: *STEP 7 Online Help.*
- Information on CPU memory reset: *Operating instructions CPU 31xC and CPU31x, Commissioning, Commissioning Modules, CPU Memory Reset by means of Mode Selector Switch*
- Evaluation of the LEDs upon error or diagnostic event: *Operating Instructions CPU 31xC and CPU 31x, Test Functions, Diagnostics and Troubleshooting, Diagnostics with the help of Status and Error LEDs*

Power supply connection

Each CPU is equipped with a double-pole power supply socket. The connector with screw terminals is inserted into this socket when the CPU is delivered.

Differences between the CPUs

Table 2-2 Differences of the CPUs 31xC

Element	CPU 312C	CPU 313C	CPU 313C-2 DP	CPU 313C-2 PtP	CPU 314C-2 DP	CPU 314C-2 PtP
9-pole DP interface (X2)	–	–	X	–	X	–
15-pole PtP interface (X2)	–	–	–	X	–	X
Digital inputs	10	24	16	16	24	24
Digital outputs	6	16	16	16	16	16
Analog inputs	–	4 + 1	–	–	4 + 1	4 + 1
Analog outputs	–	2	–	–	2	2
Technological functions	2 counters	3 counters	3 counters	3 counters	4 counters 1 channel for positioning	4 counters 1 channel for positioning

2.1.2 Status and Error Indicators: CPU 31xC

LED designation	Color	Meaning
SF	red	Hardware or software error
BF (for CPUs with DP interface only)	red	Bus error
DC5 V	green	5-V power for CPU and S7-300 bus is OK
FRCE	yellow	Force job is active
RUN	green	CPU in RUN The LED flashes during STARTUP at a rate of 2 Hz, and in HOLD state at 0.5 Hz.
STOP	yellow	CPU in STOP and HOLD or STARTUP The LED flashes at 0.5 Hz when the CPU requests a memory reset, and during the reset at 2 Hz.

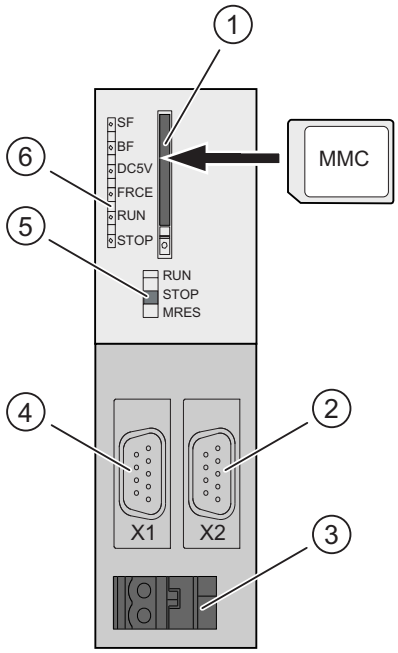
Reference

- CPU operating modes: *STEP 7 Online Help*.
- Information on CPU memory reset: *Operating instructions CPU 31xC and CPU31x, Commissioning, Commissioning Modules, CPU Memory Reset by means of Mode Selector Switch*
- Evaluation of the LEDs upon error or diagnostic event: *Operating Instructions CPU 31xC and CPU 31x, Test Functions, Diagnostics and Troubleshooting, Diagnostics with the help of Status and Error LEDs*

2.2 Operating and display elements: CPU 31x

2.2.1 Operating and display elements: CPU 312, 314, 315-2 DP:

Operating and display elements



The figures show	the following CPU elements
(1)	Slot for the SIMATIC Micro Memory Card (MMC) incl. the ejector
(2)	2. Interface X2 (only for CPU 315-2 DP)
(3)	Power supply connection
(4)	1. Interface X1 (MPI)
(5)	Mode selector switch
(6)	Status and error displays

Slot for the SIMATIC Micro Memory Card (MMC)

Memory module is a SIMATIC Micro Memory Card. You can use MMCs as load memory and as portable storage medium.

Note

These CPUs do not have an integrated load memory and thus require a SIMATIC Micro Memory Card for operation.

Mode selector switch

The mode selector switch is used to set the CPU operating mode.

Table 2-3 Mode selector switch settings

Position	Meaning	Description
RUN	RUN mode	The CPU executes the user program.
STOP	STOP mode	The CPU does not execute a user program.
MRES	CPU memory reset	Mode selector switch position with pushbutton function for CPU memory reset. A CPU memory reset by means of mode selector switch requires a specific sequence of operation.

Reference

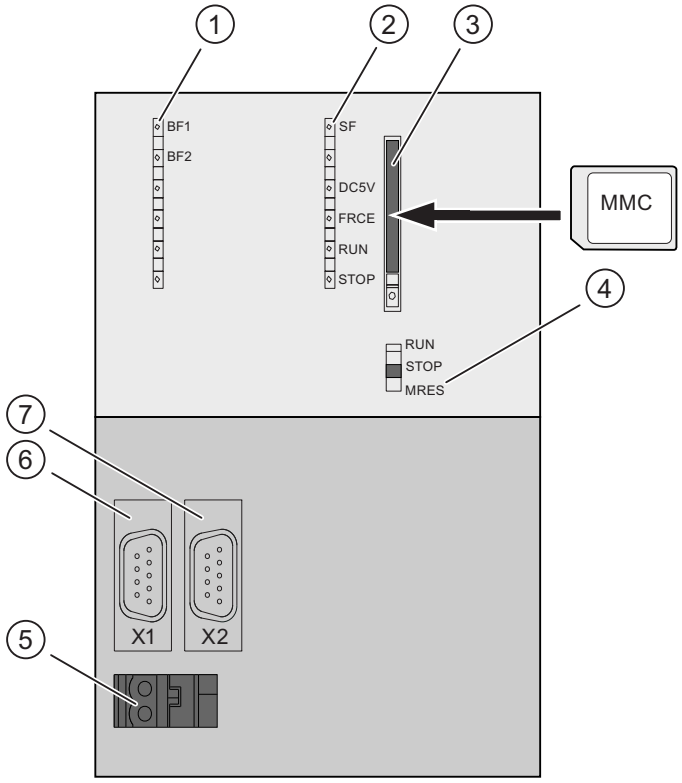
- CPU operating modes: *STEP 7 Online Help.*
- Information on CPU memory reset: *Operating instructions CPU 31xC and CPU31x, Commissioning, Commissioning Modules, CPU Memory Reset by means of Mode Selector Switch*
- Evaluation of the LEDs upon error or diagnostic event: *Operating Instructions CPU 31xC and*
  CPU 31x, Test Functions, Diagnostics and Troubleshooting, Diagnostics with the help of Status and Error LEDs

Power supply connection

Each CPU is equipped with a double-pole power supply socket. The connector with screw terminals is inserted into this socket when the CPU is delivered.

2.2.2 Operating and display elements: CPU 317-2 DP

Operating and display elements



The figures show	the following CPU elements
(1)	Bus error indicators
(2)	Status and error displays
(3)	Slot for the SIMATIC Micro Memory Card (MMC) incl. the ejector
(4)	Mode selector switch
(5)	Power supply connection
(6)	1. Interface X1 (MPI/DP)
(7)	2. Interface X2 (DP)

Slot for the SIMATIC Micro Memory Card (MMC)

Memory module is a SIMATIC Micro Memory Card. You can use MMCs as load memory and as portable storage medium.

Note

These CPUs do not have an integrated load memory and thus require a SIMATIC Micro Memory Card for operation.

Mode selector switch

Use the mode selector switch to set the CPU operating mode.

Table 2-4 Mode selector switch settings

Position	Meaning	Description
RUN	RUN mode	The CPU executes the user program.
STOP	STOP mode	The CPU does not execute a user program.
MRES	CPU memory reset	Mode selector switch position with pushbutton function for CPU memory reset. A CPU memory reset by means of mode selector switch requires a specific sequence of operation.

Reference

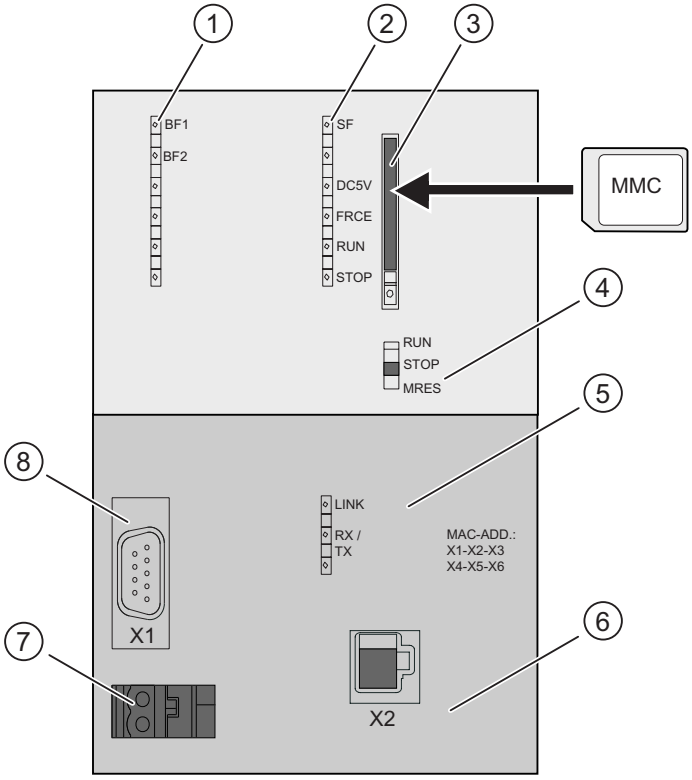
- CPU operating modes: *STEP 7 Online Help.*
- Information on CPU memory reset: *Operating instructions CPU 31xC and CPU31x, Commissioning, Commissioning Modules, CPU Memory Reset by means of Mode Selector Switch*
- Evaluation of the LEDs upon error or diagnostic event: *Operating Instructions CPU 31xC and*
  CPU 31x, Test Functions, Diagnostics and Troubleshooting, Diagnostics with the help of Status and Error LEDs

Power supply connection

Each CPU is equipped with a double-pole power supply socket. The connector with screw terminals is inserted into this socket when the CPU is delivered.

2.2.3 Operating and display elements: CPU 31x-2 PN/DP

Operating and display elements



The figures show	the following CPU elements
(1)	Bus error indicators
(2)	Status and error displays
(3)	Slot for the SIMATIC Micro Memory Card (MMC) incl. the ejector
(4)	Mode selector switch
(5)	Status display of 2nd interface (X2)
(6)	2. Interface X2 (PN)
(7)	Power supply connection
(8)	1. Interface X1 (MPI/DP)

Slot for the SIMATIC Micro Memory Card (MMC)

Memory module is a SIMATIC Micro Memory Card. You can use MMCs as load memory and as portable storage medium.

Note

These CPUs do not have an integrated load memory and thus require a SIMATIC Micro Memory Card for operation.

Mode selector switch

You can use the mode selector switch to set the current operating mode of the CPU.

Table 2-5 Mode selector switch settings

Position	Meaning	Description
RUN	RUN mode	The CPU executes the user program.
STOP	STOP mode	The CPU does not execute a user program.
MRES	CPU memory reset	Mode selector switch position with pushbutton function for CPU memory reset. A CPU memory reset by means of mode selector switch requires a specific sequence of operation.

Reference

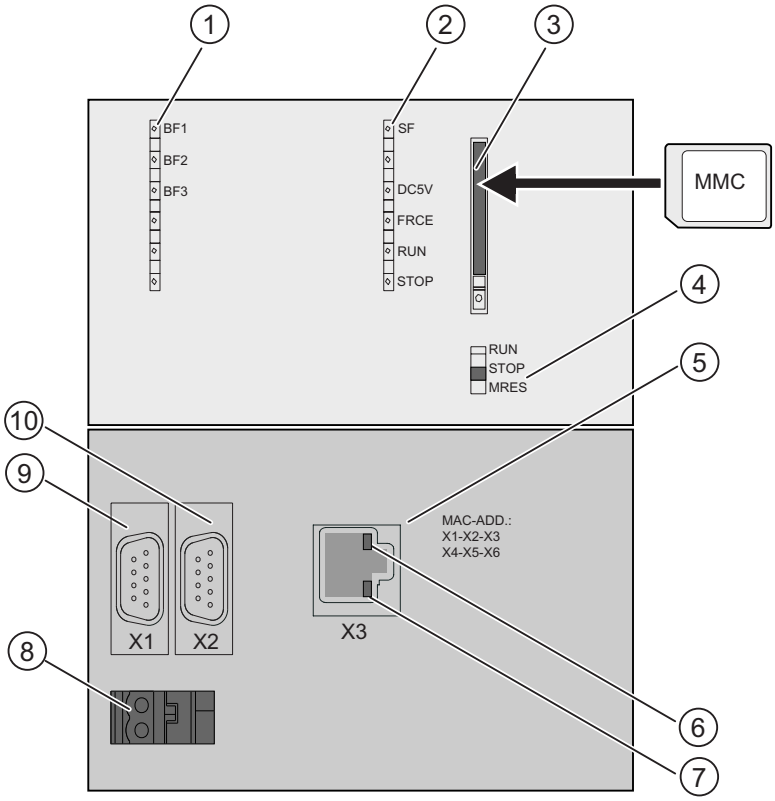
- CPU operating modes: *STEP 7 Online Help.*
- Information on CPU memory reset: *Operating instructions CPU 31xC and CPU31x, Commissioning, Commissioning Modules, CPU Memory Reset by means of Mode Selector Switch*
- Evaluation of the LEDs upon error or diagnostic event: *Operating Instructions CPU 31xC and*
  CPU 31x, Test Functions, Diagnostics and Troubleshooting, Diagnostics with the help of Status and Error LEDs

Power supply connection

Each CPU is equipped with a double-pole power supply socket. The connector with screw terminals is inserted into this socket when the CPU is delivered.

2.2.4 Operating and display elements: CPU 319-3 PN/DP

Operating and display elements



The figures show	the following CPU elements
(1)	Bus error indicators
(2)	Status and error displays
(3)	Slot for the SIMATIC Micro Memory Card (MMC) incl. the ejector
(4)	Mode selector switch
(5)	3. Interface X3 (PN)
(6)	Green LED (LED designation: LINK)
(7)	Yellow LED (LED designation: RX/TX)
(8)	Power supply connection
(9)	1. Interface X1 (MPI/DP)
(10)	2. Interface X2 (DP)

Slot for the SIMATIC Micro Memory Card (MMC)

Memory module is a SIMATIC Micro Memory Card. You can use MMCs as load memory and as portable storage medium.

Note

These CPUs do not have an integrated load memory and thus require a SIMATIC Micro Memory Card for operation.

Mode selector switch

You can use the mode selector switch to set the current operating mode of the CPU.

Table 2-6 Mode selector switch settings

Position	Meaning	Description
RUN	RUN mode	The CPU executes the user program.
STOP	STOP mode	The CPU does not execute a user program.
MRES	CPU memory reset	Mode selector switch position with pushbutton function for CPU memory reset. A CPU memory reset by means of mode selector switch requires a specific sequence of operation.

Reference

- CPU operating modes: *STEP 7 Online Help.*
- Information on CPU memory reset: *Operating instructions CPU 31xC and CPU31x, Commissioning, Commissioning Modules, CPU Memory Reset by means of Mode Selector Switch*
- Evaluation of the LEDs upon error or diagnostic event: *Operating Instructions CPU 31xC and*
  CPU 31x, Test Functions, Diagnostics and Troubleshooting, Diagnostics with the help of Status and Error LEDs

Power supply connection

Each CPU is equipped with a double-pole power supply socket. The connector with screw terminals is inserted into this socket when the CPU is delivered.

2.2.5 Status and error displays of CPU 31x

General status and error displays

Table 2-7 General status and error displays of the CPU 31x

LED designation	Color	Meaning
SF	red	Hardware or software error.
DC5 V	green	5-V power for the CPU and the S7-300 bus
FRCE	yellow	LED is lit: Active force job LED flashes at 2 Hz: Node flash test function (only CPUs with firmware V2.2.0 or higher)
RUN	green	CPU in RUN The LED flashes during STARTUP at a rate of 2 Hz, and in HOLD state at 0.5 Hz.
STOP	yellow	CPU in STOP, or HOLD, or STARTUP The LED flashes at 0.5 Hz when the CPU requests a memory reset, and during the reset at 2 Hz.

Status displays for the interfaces X1, X2 and X3

Table 2-8 Bus error displays of CPU 31x

CPU	LED designation	Color	Meaning
315-2 DP	BF	red	Bus error at DP interface (X2)
317-2 DP	BF1:	red	Bus error at interface 1 (X1)
	BF2:	red	Bus error at interface 2 (X2)
31x-2 PN/DP	BF1:	red	Bus error at interface 1 (X1)
	BF2:	red	Bus error at interface 2 (X2)
	LINK	green	Connection at interface 2 (X2) is active
	RX/TX	yellow	Receive / Transmit data at interface 2 (X2)
319-3 PN/DP	BF1:	red	Bus error at interface 1 (X1)
	BF2:	red	Bus error at interface 2 (X2)
	BF3:	red	Bus error at interface 3 (X3)
	LINK[1]	green	Connection at interface 3 (X3) is active
	RX/TX[1]	yellow	Receive / transmit data at interface 3 (X3)

[1] In the case of the CPU 319-3 PN/DP are located directly at the RJ45 socket (LEDs are not labeled!)

Reference

- CPU operating modes: *STEP 7 Online Help.*
- Information on CPU memory reset: *Operating instructions CPU 31xC and CPU31x, Commissioning, Commissioning Modules, CPU Memory Reset by means of Mode Selector Switch*
- Evaluation of the LEDs upon error or diagnostic event: *Operating Instructions CPU 31xC and*
  CPU 31x, Test Functions, Diagnostics and Troubleshooting, Diagnostics with the help of Status and Error LEDs

Communication 3

3.1 Interfaces

3.1.1 Multi-Point Interface (MPI)

Availability

All the CPUs described here are equipped with an MPI interface

A CPU equipped with an MPI/DP interface is configured and supplied as MPI interface. To use the DP interface, set DP interface mode in STEP 7.

Properties

The MPI (Multi-Point Interface) represents the CPU interface for PG/OP connections, or for communication on an MPI subnet.

The typical (default) transmission rate of all CPUs is 187.5 kbps. You can also set 19.2 kbps for communication with an S7-200. Baud rates of up to 12 Mbaud are possible with the CPU 315-2 PN/DP, CPU 317 and CPU 319-3 PN/DP.

The CPU automatically broadcasts its bus configuration via the MPI interface (the transmission rate, for example). A PG, for example, can thus receive the correct parameters and automatically connect to a MPI subnet.

Note

You may only connect PGs to an MPI subnet which is in RUN.
Other stations (for example, OP, TP, ...) should not be connected to the MPI subnet while the system is in RUN. Otherwise, transferred data might be corrupted as a result of interference, or global data packages may be lost.

Devices capable of MPI communication

- PG/PC
- OP/TP
- S7-300 / S7-400 with MPI interface
- S7-200 (19.2 kbps only)

3.1.2 PROFIBUS DP

Availability

CPUs with the "DP" have at least one DP interface.

The 315-2 PN/DP and 317 CPUs are equipped with an MPI/DP interface.
The CPU319-3 PN/DP has an MPI/DP interface and additionally a DP interface. A CPU with MPI/DP interface is supplied with a default MPI configuration. You need to set DP mode in STEP 7 if you want to use the DP interface.

Operating modes for CPUs with two DP interfaces

Table 3-1 Operating modes for CPUs with two DP interfaces

MPI/DP interface	PROFIBUS DP interface
• MPI	• not configured
• DP master	• DP master
• DP slave [1]	• DP slave [1]

[1] simultaneous operation of the DP slave on both interfaces is excluded

Properties

The PROFIBUS DP interface is mainly used to connect distributed I/O. PROFIBUS DP allows you to create large subnets, for example.

The PROFIBUS DP interface can be set for operation in master or slave mode, and supports transmission rates up to 12 Mbps.

The CPU broadcasts its bus parameters (transmission rate, for example) via the PROFIBUS DP interface when master mode is set. A PG, for example, can thus receive the correct parameters and automatically connect to a PROFIBUS subnet. In your configuration you can specify to disable bus parameter broadcasting.

Note

(for DP interface in slave mode only)

When you disable the Commissioning / Debug mode / Routing check box in the DP interface properties dialog in STEP 7, all user-specific transmission rate settings will be ignored, and the transmission rate of the master is automatically set instead. This disables the routing function at this interface.

Devices capable of PROFIBUS DP communication

- PG/PC
- OP/TP
- DP slaves
- DP master
- Actuators/Sensors
- S7-300/S7-400 with PROFIBUS DP interface

Reference

Further information on PROFIBUS: http://www.profibus.com

3.1.3 PROFINET (PN)

Availability

CPUs with a "PN" name suffix are equipped with a PROFINET interface.

Connecting to Industrial Ethernet

You can use the integrated PROFINET interface of the CPU to establish a connection to Industrial Ethernet.

The integrated PROFINET interface of the CPU can be configured via MPI or PROFINET.

Devices capable of PROFINET (PN) communication

- PROFINET IO devices (for example, interface module IM 151-3 PN in an ET 200S)
- S7-300 / S7-400 with PROFINET interface (for example, CPU 317-2 PN/DP or CP 343-1)
- Active network components (a switch, for example)
- PG/PC with network card

Properties of the PROFINET interface

Properties	
IEEE standard	802.3
Connector design	RJ45
Transmission speed	Max. 100 Mbps
Media	Twisted Pair Cat5 (100BASE-TX)

Note

Networking PROFINET components

The use of switches, rather than hubs, for networking PROFINET components brings about a substantial improvement in decoupling bus traffic, and improves runtime performance under higher bus load. PROFINET CBA with cyclic PROFINET interconnections requires the use of switches in order to maintain compliance with performance specifications. Full duplex mode at 100 Mbps is mandatory for cyclic PROFINET interconnections.

PROFINET IO also requires the use of switches and 100 Mbps full duplex mode.

Reference

- For instructions on how to configure the integrated PROFINET interface, refer to *S7-300, CPU 31xC and CPU 31x operating instructions (Setup)*.
- For further information on PROFINET, refer to *PROFINET System Description*
- For detailed information on Ethernet networks, network configuration and network components refer to the *SIMATIC NET Manual: Twisted-Pair and Fiber Optic Networks* , available under article ID 8763736 at http://support.automation.siemens.com.
- *Component Based Automation, Commissioning SIMATIC iMap Systems - Tutorial,* Article ID 18403908
- Further information about PROFINET: http://www.profinet.com

See also

PROFINET IO System (Page 3-19)

3.1.4 Point to Point (PtP)

Availability

CPUs with the "PtP" name suffix have at least one PtP interface.

Properties

Using the PtP interface of your CPU, you can connect external devices with serial interface. You can operate such a system at transmission rates up to 19.2 kbps in full duplex mode (RS 422), and up to 38.4 kbps in half duplex mode (RS 485).

Transmission rate

- Half duplex: 38.4 kbps
- Full duplex: 19.2 kbps

Drivers

PtP communication drivers installed in those CPUs:

- ASCII drivers
- 3964(R) Protocol
- RK 512 (CPU 314C-2 PtP only)

Devices capable of PtP communication

Devices equipped with a serial port, for example, barcode readers, printers, etc.

Reference

CPU 31xC: Technological functions manual

3.2 Communication services

3.2.1 Overview of communication services

Selecting the communication service

You need to decide on a communication service, based on functionality requirements. Your choice of communication service will have no effect on:

- the functionality available,
- whether an S7 connection is required or not, and
- the time of connecting.

The user interface can vary considerably (SFC, SFB, ...), and is also determined by the hardware used (SIMATIC CPU, PC, ...).

Overview of communication services

The table below provides an overview of communication services offered by the CPUs.

Table 3-2 Communication services of the CPUs

Communication service	Functionality	Time at which the S7 connection is established ...	via MPI	via DP	via PtP	via PN
PG communication	Commissioning, test, diagnostics	From the PG, starting when the service is being used	X	X	–	X
OP communication	Monitor and modify	via OP at POWER ON	X	X	–	X
S7 basic communication	Data exchange	is programmed at the blocks (SFC parameters)	X	–	–	–
S7 communication	Data exchange in server and client mode: Configuration of communication required.	via active partner at POWER ON.	Only in server mode	Only in server mode	–	X
Global data communication	Cyclic data exchange (for example, flag bits)	does not require an S7 connection	X	–	–	–
Routing PG functions (only for CPUs with DP or PN interface)	for example testing, diagnostics on other networks also	from the PG, starting when the service is being used	X	X	–	X
PtP communication	Data exchange via serial interface	does not require an S7 connection	–	–	X	–
PROFIBUS DP	Data exchange between master and slave	does not require an S7 connection	–	X	–	–
PROFINET CBA	Data exchange by means of component based communication	does not require an S7 connection	–	–	–	X

Communication service	Functionality	Time at which the S7 connection is established ...	via MPI	via DP	via PtP	via PN
PROFINET IO	Data exchange between IO controllers and the IO devices	does not require an S7 connection	–	–	–	X
SNMP (Simple Network Management Protocol)	Standard protocol for network diagnostics and configuration	does not require an S7 connection	–	–	–	X
open communication by means of TCP/IP	Data exchange via Industrial Ethernet with TCP/IP protocol (by means of loadable FBs)	Does not require an S7 connection, is handled in the user program by means of loadable FBs	–	–	–	X
Open communication by means of ISO on TCP	Data exchange via Industrial Ethernet with ISO-on-TCP protocol (by means of loadable FBs)	Does not require an S7 connection, is handled in the user program by means of loadable FBs	–	–	–	X
Open communication by means of UDP	Data exchange via Industrial Ethernet with UDP protocol (by means of loadable FBs)	Does not require an S7 connection, is handled in the user program by means of loadable FBs	–	–	–	X

See also

Distribution and availability of S7 connection resources (Page 3-30)

Connection resources for routing (Page 3-32)

3.2.2 PG communication

Properties

PG communication is used to exchange data between engineering stations (PG, PC, for example) and SIMATIC modules which are capable of communication. This service is available for MPI, PROFIBUS and Industrial Ethernet subnets. Transition between subnets is also supported.

PG communication provides the functions needed to download / upload programs and configuration data, to run tests and to evaluate diagnostic information. These functions are integrated in the operating system of
SIMATIC S7 modules.

A CPU can maintain several simultaneous online connections to one or multiple PGs.

3.2.3 OP communication

Properties

OP communication is used to exchange data between operator stations (OP, TP, for example) and SIMATIC modules which are capable of communication. This service is available for MPI, PROFIBUS and Industrial Ethernet subnets.

OP communication provides functions you require for monitoring and modifying. These functions are integrated in the operating system of SIMATIC S7 modules. A CPU can maintain several simultaneous connections to one or several OPs.

3.2.4 Data exchanged by means of S7 basic communication

Properties

S7-based communication is used to exchange data between S7 CPUs and the communication-capable SIMATIC modules within an S7 station (acknowledged data exchange). Data are exchanged across non-configured S7 connections. The service is available via MPI subnet, or within the station to function modules (FM).

S7-based communication provides the functions you require for data exchange. These functions are integrated into the CPU operating system. The user can utilize this service by means of "System function" (SFC) user interface.

Reference

Further information

- on SFCs, refer to *Instruction list.*
  For further information refer to *STEP 7 Online Help* or *System and Standard Functions* reference manual.
- on communication can be found in the *Communication with SIMATIC* manual.

3.2.5 S7 communication

Properties

A CPU can always operate in server or client mode in S7 communication: We distinguish between

- communication with unilateral configuration (for PUT/GET only)
- communication with bilateral configuration (for USEND, URCV, BSEND, BRCV, PUT, GET)

However, the functionality depends on the CPU. A CP is therefore required in certain situations.

Table 3-3 Client and server in S7 communication, using connections with unilateral / bilateral configuration

CPU	Use in server mode for connections with unilateral configuration	Use in server mode for connections with bilateral configuration	Use as client
31xC >= V1.0.0	Generally possible on MPI/DP interface without configuration of user interface	Only possible with CP and loadable FBs.	Only possible with CP and loadable FBs.
31x >= V2.0.0	Generally possible on MPI/DP interface without configuration of user interface	Only possible with CP and loadable FBs.	Only possible with CP and loadable FBs.
31x >= V2.2.0	Generally possible on MPI/DP/PN interface without configuration of user interface	• Possible on PN interface with loadable FBs or • with CP and loadable FBs.	• Possible on PN interface with loadable FBs or • with CP and loadable FBs.

The user interface is implemented using standard function modules (FBs) from the standard library of STEP 7, under communication blocks.

Reference

For further information on communication, refer to the *Communication with SIMATIC* manual.

3.2.6 Global data communication (MPI only)

Properties

Global data communication is used for cyclic exchange of global data via MPI subnets (for example, I, Q, M) between SIMATIC S7 CPUs (data exchange without acknowledgement). One CPU broadcasts its data to all other CPUs on the MPI subnet. This function is integrated in the CPU operating system.

Reduction ratio

The reduction ratio specifies the cyclic intervals for GD communication. You can set the reduction ratio when you configure global data communication in STEP 7. For example, if you set a reduction ratio of 7, global data are transferred only with every 7th cycle. This reduces CPU load.

Send and receive conditions

Conditions which should be satisfied for GD communication:

- For the transmitter of a GD packet:
  Reduction ratio$_{transmitter}$ x cycle time$_{transmitter}$ ≥ 60 ms
- For the receiver of a GD packet:
  Reduction ratio$_{receiver}$ x cycle time$_{receiver}$
  < reduction ratio$_{transmitter}$ x cycle time$_{transmitter}$

A GD packet may be lost if you do not adhere to these conditions. The reasons being:

- the performance of the "smallest" CPU in the GD circuit
- asynchronous transmitting / receiving of global data at the stations

When setting in STEP 7: “Transmit after each CPU cycle“, and the CPU has a short scan cycle time (< 60 ms), the operating system might overwrite a GD packet of the CPU before it is transmitted. The loss of global data is indicated in the status box of a GD circuit, if you set this function in your STEP 7 configuration.

GD resources of the CPUs

Table 3-4 GD resources of the CPUs

Parameters	CPU 31xC, 312, 314	CPU 315-2 DP, 315-2 PN/DP, 317-2 DP, 317-2 PN/DP, 319-3 PN/DP
Number of GD circuits per CPU	Max. 4	Max. 8
GD packets transmitted per GD circuit	Max. 1	Max. 1
GD packets transmitted by all GD circuits	Max. 4	Max. 8
GD packets received per GD circuit	Max. 1	Max. 1
GD packets received by all GD circuits	Max. 4	Max. 8
Data length per GD packet	Max. 22 bytes	Max. 22 bytes
Consistency	Max. 22 bytes	Max. 22 bytes
Min. reduction ratio (default)	1 (8)	1 (8)

3.2.7 Routing

Properties

STEP 7 V5.1 + SP4 or higher allows you to access your S7 stations on all subnets with your PG/PC, for example, to

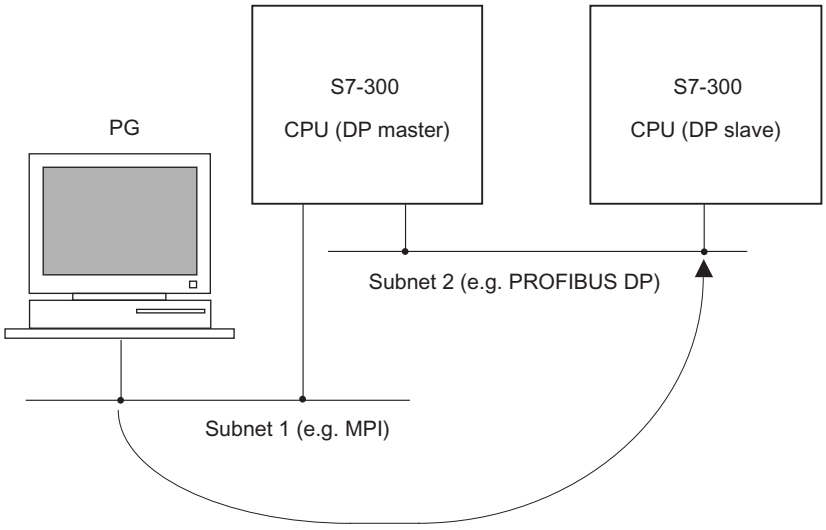
- download user programs
- download a hardware configuration, or
- perform debugging and diagnostic functions.

Note

If you use your CPU as I-slave, the routing function is only possible when the DP interface is switched to active IN STEP 7, set the Test, Commission Routing check box on the properties dialog of the DP interface. For detailed information, refer to the *Programming with STEP 7* manual, or directly to the *STEP 7 Online Help*

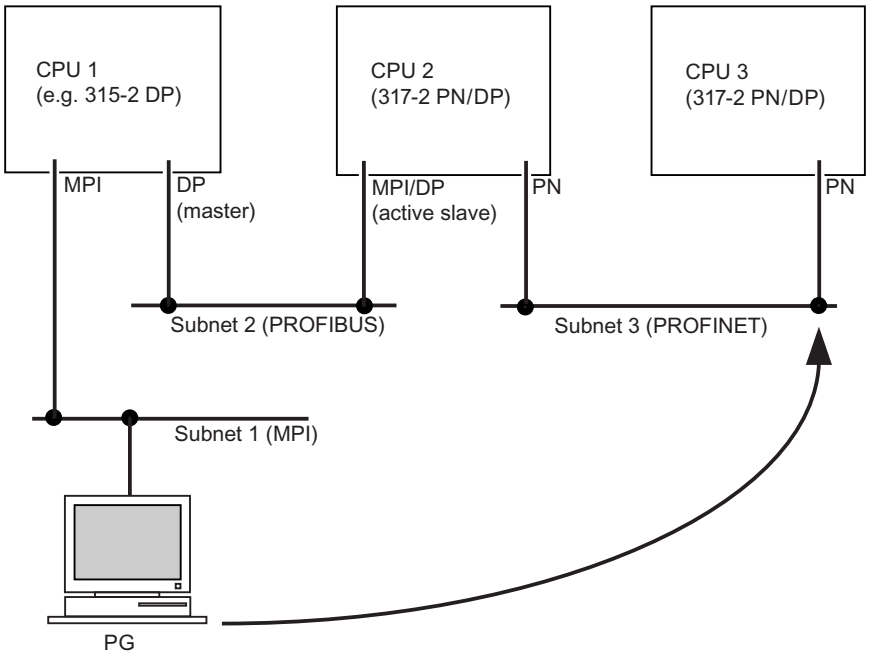
Routing network nodes: MPI - DP

Gateways between subnets are routed in a SIMATIC station that is equipped with interfaces to the respective subnets. The figure below shows CPU 1 (DP master) acting as router for subnets 1 and 2.



The figure below shows the MPI access to PROFINET via PROFIBUS CPU 1 (315-2 DP, for example) is the router for subnet 1 and 2;
CPU 2 is the router for subnet 2 and 3.

Routing network nodes: MPI - DP - PROFINET



Number of connections for routing

The CPUs with DP interface provide a different number of connections for the routing function:

Table 3-5 Number of routing connections for DP CPUs

CPU	As of firmware version	Number of connections for routing
31xC, CPU 31x	2.0.0	Max. 4
317-2 DP	2.1.0	Max. 8
31x-2 PN/DP	2.2.0	Interface X1 configured as: • MPI: Max. 10 • DP master: Max. 24 • DP slave (active): Max. 14 Interface X2 configured as: • PROFINET: Max. 24
319-3 PN/DP	2.4.0	Interface X1 configured as: • MPI: Max. 10 • DP master: Max. 24 • DP slave (active): Max. 14 Interface X2 configured as: • DP master: Max. 24 • DP slave (active): Max. 14 Interface X3 configured as: • PROFINET: Max. 48

Requirements

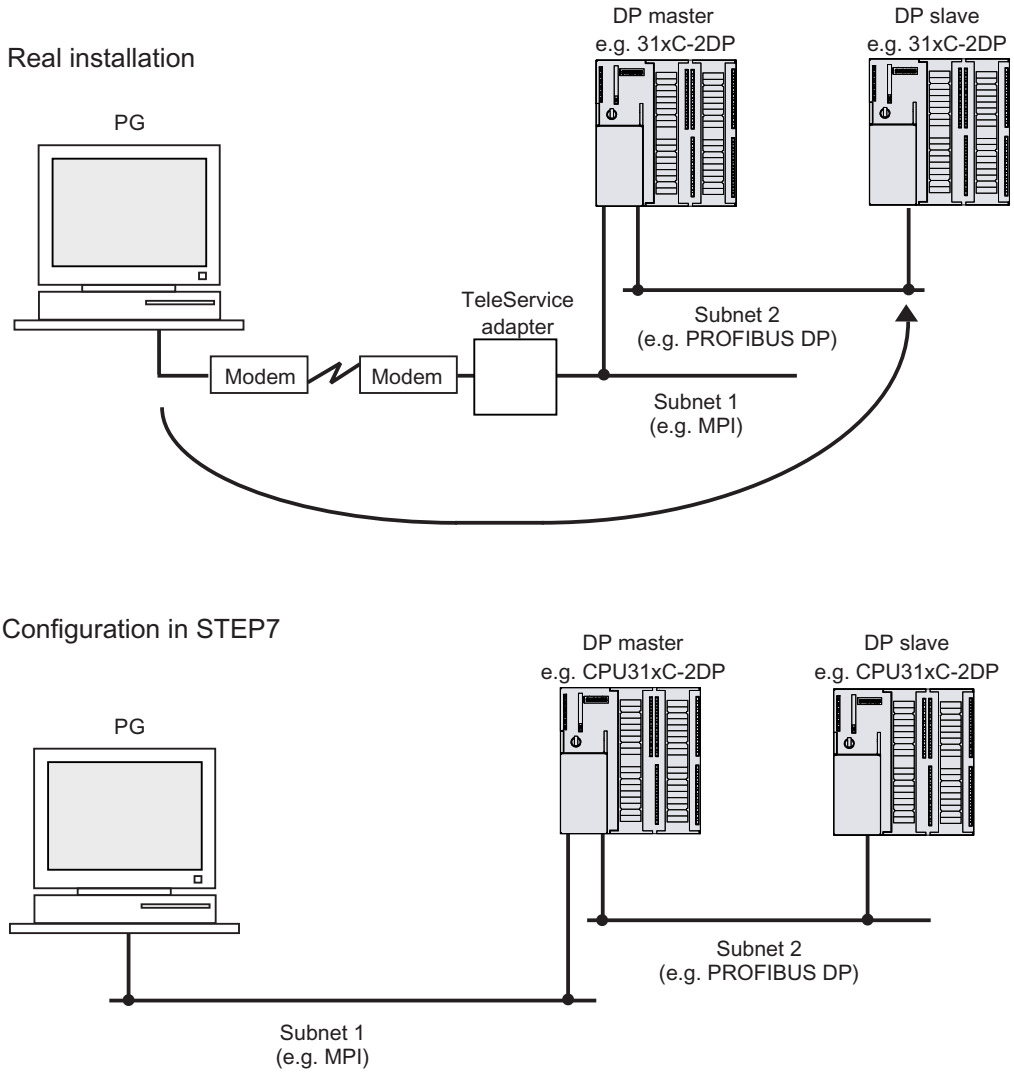
- The station modules are "capable of routing" (CPUs or CPs).
- The network configuration does not exceed project limits.
- The modules have loaded the configuration data containing the latest "knowledge" of the entire network configuration of the project.

  Reason: All modules participating in the network transition must receive the routing information defining the paths to other subnets.
- In your network configuration, the PG/PC you want to use to establish a connection via network node must be assigned to the network it is physically connected to.
- The CPU must set to master mode, or
- when set to operate in slave mode, the Test, Commissioning, Routing functionality must be enabled by setting the check box in STEP 7, in the DP interface for DP slave properties dialog box.

Routing: Example of a TeleService application

The figure below shows the example of an application for remote maintenance of an S7 station using a PG. The connection to other subnets is here established via modem connection.

The lower section of the figure shows how to configure this in STEP 7.



Reference

Further information

- on configuring in STEP 7 is found in the *Configuring Hardware and Connections in STEP 7* manual
- of a basic nature is contained in the *Communication with SIMATIC* Manual.
- about the TeleService adapter is available under article ID 20983182 on the Internet URL http://support.automation.siemens.com.
- on SFCs, refer to *Instruction list*.
  For further information refer to *STEP 7 Online Help* or *System and Standard Functions* reference manual.
- on communication are found in the *Communication with SIMATIC* Manual.

3.2.8 Point-to-point connection

Properties

PtP communication enables you to exchange data via serial port. PtP communication can be used to interconnect automation devices, computers or communication-capable systems of external suppliers. The function also allows adaptation to the protocol of the communication partner.

Reference

Further Information

- on SFCs are found in the *Instruction list*.
  For detailed information, refer to the *STEP 7 Online Help* , or to the *System and Standard Functions* Reference Manual.
- on communication are found in the *Communication with SIMATIC* Manual.

3.2.9 Data consistency

Properties

A data area is consistent if it can be read or written to from the operating system as a consistent block. Data exchanged collectively between the stations should belong together and originate from a single processing cycle, that is, be consistent. If the user program contains a programmed communication function, for example, access to shared data with X-SEND/ XRCV, access to that data area can be coordinated by means of the "BUSY" parameter itself.

With PUT/GET functions

For S7 communication functions, such as PUT/GET or write / read via OP communication, which do not require a block in the user program on the CPU (operating in server mode), allowances must be made in the program for the extent of the data consistency. The PUT/GET functions for S7 communication, or for reading/writing variables via OP communication, are executed at the CPU's scan cycle checkpoint. To save a defined process alarm response time, the communication variables are copied in blocks of up to 64 bytes (CPU 317, CPU 319: 160 bytes) to / from work memory at the scan cycle checkpoint of the operating system. Data consistency is not guaranteed for larger data areas.

Note

If a defined data deficiency is required, the defined communication variables in the user program of the CPU may be no larger than 64 bytes (for CPU 317, CPU 319: 160 bytes.)

3.2.10 Communication by means of PROFINET

What is PROFINET?

Within the framework of Totally Integrated Automation (TIA), PROFINET represents a consequent enhancement of:

- PROFIBUS DP, the established fieldbus and
- Industrial Ethernet, the communication bus for the cell level

Experience gained from both systems was and is being integrated into PROFINET.

PROFINET is an Ethernet-based automation standard of PROFIBUS International (previously PROFIBUS Users Organization e.V.), and defines a multi-vendor communication, automation, and engineering model.

Objectives in PROFINET

The objectives in PROFINET are:

- Open Ethernet Standard for automation based on Industrial Ethernet.
  Although Industrial Ethernet and Standard Ethernet components can be used together, the Industrial Ethernet devices are more sturdy and therefore better suited for industrial environments (temperature, immunity to interference, etc.)
- Use of TCP/IP and IT standards
- Automation with real-time Ethernet
- Total integration of field bus systems

Implementation of PROFINET by us

We have integrated PROFINET as follows:

- We have implemented communication between field devices with **PROFINET IO**.
- We have implemented communication between controllers as components in distributed systems with **PROFINET CBA** (Component based Automation)
- Installation engineering and network components are available in SIMATIC NET.
- Established IT standards from the Office environment (e.g. SNMP=Simple Network Management Protocol for network parameter assignment and diagnosis) are used for remote maintenance and network diagnostics.

Documentation from PROFIBUS International on the Internet

Numerous texts on the subject of PROFINET are available from the URL "http://www.profinet.com" from PROFIBUS International (formerly PROFIBUS Nutzer-Organisation, PNO)

For further information, refer to Internet address " http://www.siemens.com\profinet\".

What is PROFINET IO?

Within the framework of PROFINET, PROFINET IO is a communication concept for the implementation of modular, distributed applications.

PROFINET IO allows you to create automation solutions, which are familiar to you from PROFIBUS.

That is, you have the same application view in STEP 7, regardless of whether you configure PROFINET or PROFIBUS devices.

What is PROFINET CBA (Component Based Automation)?

Within the framework of PROFINET, PROFINET CBA is an automation concept for the implementation of applications with distributed intelligence.

PROFINET CBA lets you create distributed automation solutions, based on default components and partial solutions.

Component-based Automation allows you to use complete technological modules as standardized components in large systems.

The components are also created in an engineering tool which may differ from vendor to vendor. Components of SIMATIC devices are created, for example, with STEP 7.

Extent of PROFINET CBA and PROFINET IO

PROFINET IO and CBA represent two different views of automation devices on Industrial Ethernet.

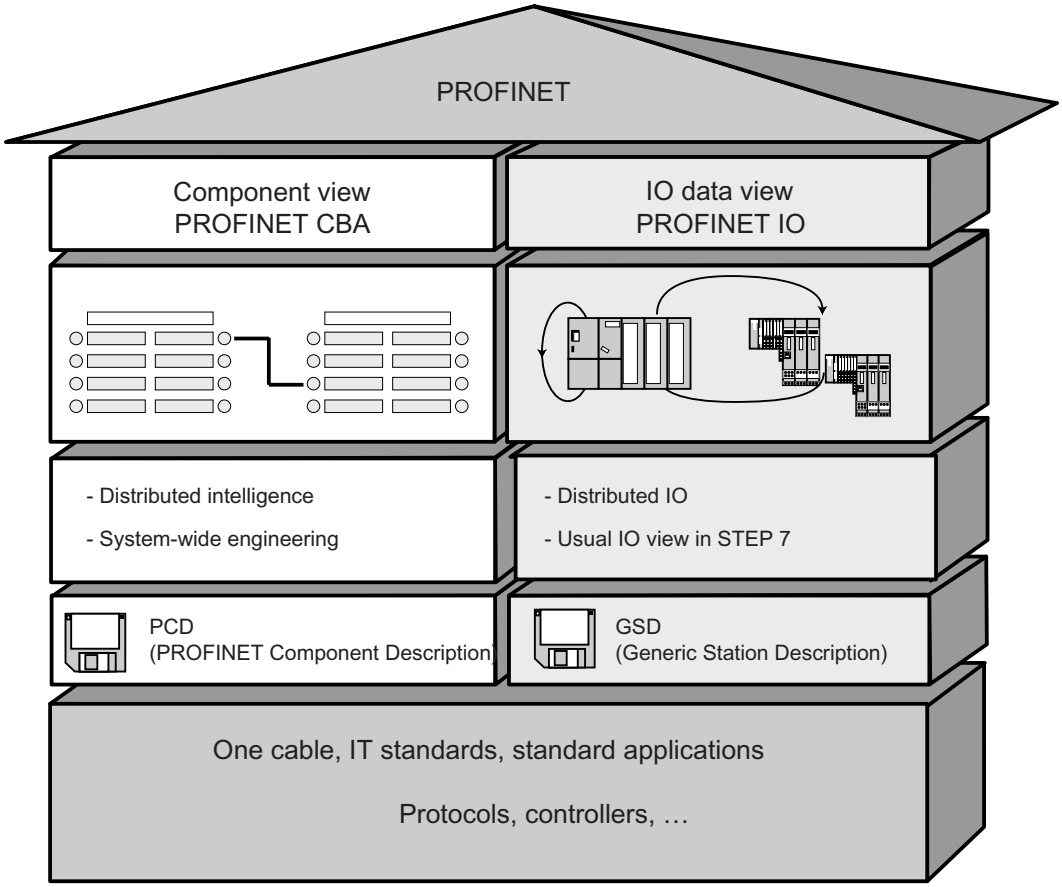


Figure 3-1 Extent of PROFINET IO and Component-Based Automation

Component Based Automation divides the entire system into various functions. These functions are configured and programmed.

PROFINET IO provides you with a view of the system that is very similar to the view obtained in PROFIBUS. You continue to configure and program the individual automation devices.

Reference

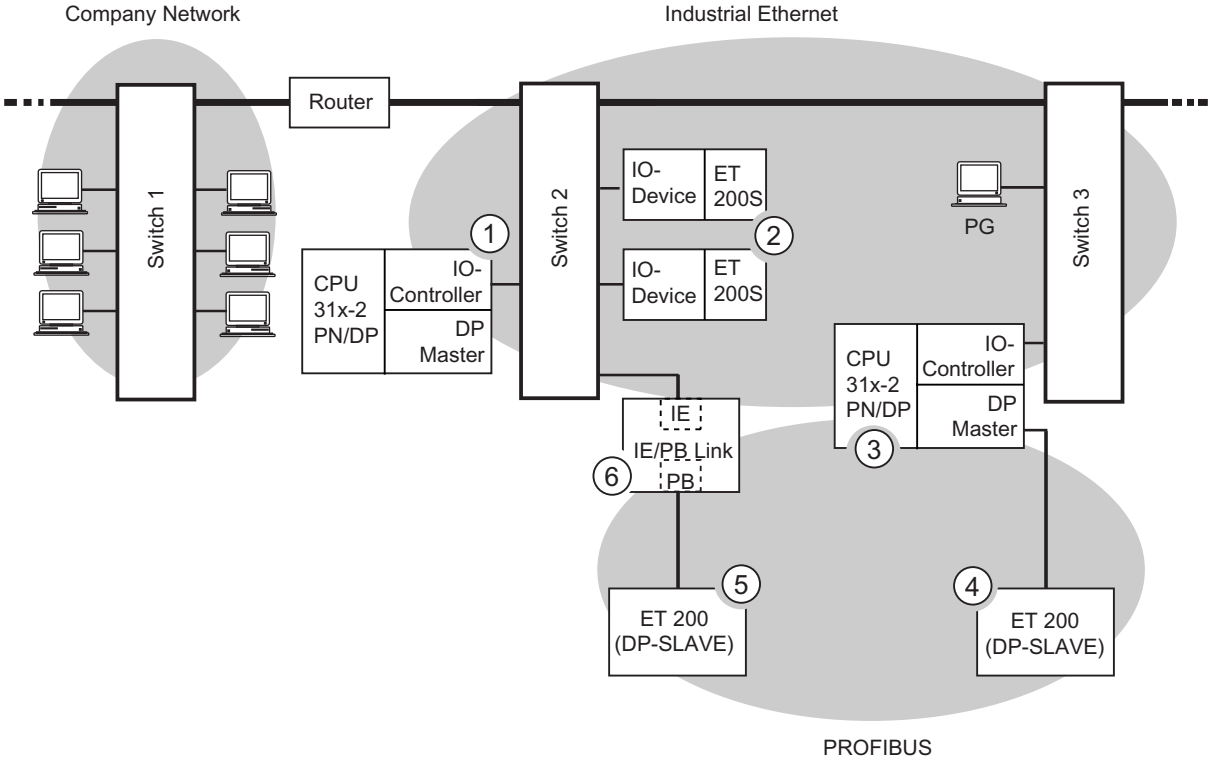
Further Information

- on PROFINET IO and PROFINET CBA is available in the *PROFINET system specification.*
  For differences and similarities between PROFIBUS DP and PROFINET IO, refer to the *From PROFIBUS DP to PROFINET IO* programming manual.
- For further information about PROFINET CBA, refer to the documentation on SIMATIC iMAP and Component Based Automation.

3.2.10.1 PROFINET IO System

Extended Functions of PROFINET IO

The following graphic shows the new functions of PROFINET IO



The graphic displays	Examples of connection paths
The connection of company network and field level	From PCs in your company network, you can access devices at the field level Example: • PC - Switch 1 - Router - Switch 2 - CPU 31x PN/DP ①.
The connection between the automation system and field level	You can, of course, also access one of the other areas in Industrial Ethernet from an IO supervisor at the field level. Example: • IO supervisor - Switch 3 - Switch 2 - ET 200S IO device ②.
The IO controller of the CPU 31x PN/DP ① **directly** controls devices on the Industrial Ethernet and on the PROFIBUS	At this point, you see the extended IO feature between the IO controller and IO device(s) on Industrial Ethernet: • The CPU 31x PN/DP ①is the IO controller for one of the ET 200S ② IO-Devices. • Die CPU 31x PN/DP ① is via the IE/PB Link ⑥ also the IO controller for the ET 200 (DP slave) ⑤.
A CPU can be both IO controller and DP master.	Here, you can see that a CPU can be both IO controller for an IO device as well as DP master for a DP slave: • The CPU 31x PN/DP ③ is the IO controller for the the other ET 200S ② IO device. CPU 31x PN/DP ③ - Switch 3 - Switch 2 - ET 200S ② • The CPU 31x PN/DP ③ is the DP master for a DP slave ④. The DP slave ④ is assigned locally to the CPU ③ and is not visible on Industrial Ethernet.

Reference

For information

- on PROFINET refer to the *From PROFIBUS DP to PROFINET IO programming manual.* This manual also provides a comprehensive overview of the new PROFINET blocks and system status lists.

See also

PROFINET (PN) (Page 3-3)

3.2.10.2 Blocks in PROFINET IO

Content of this Section

This section explains the following:

- Which blocks are intended for PROFINET
- Which blocks are intended for PROFIBUS DP
- Which blocks are intended for both PROFINET IO and PROFIBUS DP

Compatibility of the New Blocks

For PROFINET IO, it was necessary to create some new blocks, among other things, because larger configurations are now possible with PROFINET. You can also use the new blocks with PROFIBUS.

Comparison of the System and Standard Functions of PROFINET IO and PROFIBUS DP

For CPUs with an integrated PROFINET interface, the table below provides you with an overview of:

- System and standard functions for SIMATIC that you may need to replace when converting from PROFIBUS DP to PROFINET IO.
- New system and standard functions

Table 3-6 New System and Standard Functions/System and Standard Functions to be Replaced

Blocks	PROFINET IO	PROFIBUS DP
SFC 12 (deactivation and activation of DP slaves/IO devices)	Yes (as of firmware V.2.4.0)	Yes
SFC 13 (read diagnostic data of a DP slave)	No Substitute: • event-related: SFB 54 • state-related: SFB 52	Yes
SFC 58/59 (write/read data record in I/O)	No (replacement: SFB 53/52)	Yes (but should already have been replaced by SFB 53/52 in DPV1)

Blocks	PROFINET IO	PROFIBUS DP
SFB 52/53 (read/write data record)	Yes	Yes
SFB 54 (evaluate interrupt)	Yes	Yes
SFC102 (read predefined parameters)	No (replacement: SFB81)	Yes
SFB 81 (read predefined parameters)	Yes	Yes
SFC5 (query start address of a module)	No (replacement: SFC70)	Yes
SFC 70 (query start address of a module)	Yes	Yes
SFC49 (query the slot belonging to a logical address)	No (replacement: SFC71)	Yes
SFC 71 (query the slot belonging to a logical address)	Yes	Yes

The following table provides you with an overview of the system and standard functions for SIMATIC, whose functionality must be implemented by other functions when converting from PROFIBUS DP to PROFINET IO.

Table 3-7 System and Standard Functions in PROFIBUS DP that must be Implemented with Different Functions in PROFINET IO

Blocks	PROFINET IO	PROFIBUS DP
SFC 55 (write dynamic parameters)	No (simulate via SFB 53)	Yes
SFC 56 (write predefined parameters)	No (simulate via SFB 81 and SFB 53)	Yes
SFC 57 (assign module parameters)	No (simulate via SFB 81 and SFB 53)	Yes

You cannot use the following SIMATIC system and standard functions with PROFINET IO:

- SFC 7 (trigger hardware interrupt on DP master)
- SFC 11 (synchronize groups of DP slaves)
- SFC 72 (read data from a communication partner within local S7 station)
- SFC 73 (write data to a communication partner within local S7 station)
- SFC 74 (abort an existing connection to a communication partner within local S7 station)
- SFC 103 (determine the bus typology in a DP master)

Comparison of the Organization Blocks of PROFINET IO and PROFIBUS DP

Here, there are changes in OB 83 and OB 86, as shown in the following table.

Table 3-8 OBs in PROFINET IO and PROFIBUS DP

Blocks	PROFINET IO	PROFIBUS DP
OB 83 (removing and inserting modules during operation)	Also possible with an S7-300, new error information	With an S7-300 **not** possible Removing and inserting modules during operation is reported by slaves added using a GSD file by means of a diagnostic interrupt; in other words OB 82. In the case of S7 slaves, a swapping interrupt causes a station failure to be reported and OB 86 to be called.
OB 86 (rack failure)	New error information	Unchanged

Detailed Information

For detailed descriptions of the individual blocks, refer to the manual *System Software for S7-300/400 System and Standard Functions*.

3.2.10.3 System status lists (SSLs) in PROFINET IO

Content of this Section

This section explains the following:

- Which system status lists are intended for PROFINET IO
- Which system status lists are intended for PROFIBUS DP
- Which system status lists are intended for both PROFINET IO and PROFIBUS DP

Introduction

The CPU of the SIMATIC modules can provide you with certain information. The CPU stores this information in the "system status list".

The system status list describes the current status of the automation system. It provides an overview of the configuration, the current parameter assignment, the current statuses and sequences in the CPU, and the assigned modules.

The system status list data are read-only; they cannot be changed. The system status list is a virtual list that is compiled only on request.

With the help of a system status list you receive the following information via the PROFINET IO system:

- System data
- Module status information in the CPU
- Diagnostic data on module
- Diagnostic buffer

Compatibility of the New System Status Lists

For PROFINET IO, the system status lists had to be revamped to some extent because, among other things, larger configurations are now possible with PROFINET.

You should also use these new system status lists with PROFIBUS.

You can continue to use a known PROFIBUS system status list that is also supported by PROFINET. If you use a system status list in PROFINET that PROFINET does not support, an error code is returned in RET_VAL (8083: Index wrong or not permitted).

Comparison of the System Status Lists of PROFINET IO and PROFIBUS DP

Table 3-9 Comparison of the System Status Lists of PROFINET IO and PROFIBUS DP

SSL-ID	PROFINET IO	PROFIBUS DP	Applicability
W#16#0591	yes (parameter adr1 changed)	Yes	Module status information for the interfaces of a module
W#16#0A91	Yes (parameter adr1 changed)	Yes	Status information of all subsystems and master systems (S7-300 without CPU 318-2 DP)
W#16#0C91	Yes (parameter adr1/adr2 and set/actual type identifier changed)	Yes	Module status information of a module in a central configuration or attached to an integrated DP or PN interface module using the logical address of the module.
W#16#4C91	Yes (parameter adr1 changed)	Yes	Not with S7-300 Module status information of a module attached to an external DP or PN interface module using the start address
W#16#0D91	Yes (parameter adr1 changed)	Yes	Module status information of all modules in the specified rack/station
W#16#0696	Yes	No	Module status information of all submodules of a module using the logical address of the module, not possible for submodule 0 (= module)
W#16#0C96	Yes	Yes	Module status information of a submodule using the logical address of this submodule
W#16#xy92	No (replacement: SSL-ID W#16#0x94)	Yes	Rack/stations status information Replace this system status list with the system status list with ID W#16#xy94 in PROFIBUS DP, as well.
W#16#0x94	Yes	Yes	Rack/station status information

Detailed Information

For detailed descriptions of the individual system status lists, refer to the manual *System Software for S7-300/400 System and Standard Functions*.

3.2.10.4 Open communication via Industrial Ethernet

Requirements

- STEP 7 V5.3 + Servicepack 1 or higher

Functionality

The CPUs with integrated PROFINET interface as of firmware V2.3.0 or V2.4.0 support the functionality of open communication by means of Industrial Ethernet (abbreviated: *open IE communication*)

Following services are available for open IE communication:

- Connection oriented protocols
  - TCP native according to RFC 793, connection type B#16#01, as of firmware V2.3.0
  - TCP native according to RFC 793, connection type B#16#11, as of firmware V2.4.0
  - ISO on TCP according to RFC 1006, as of firmware V2.4.0
- Connectionless protocols
  - UDP according to RFC 768, as of firmware V2.4.0

Features of the communication protocols

The following distinctions are made between protocol types in data communication:

- Connection oriented protocols:

  Prior to data transmission these establish a (logical) connection to the communication partner and close this again, if necessary, after transmission is completed. Connection oriented protocols are used when security in especially important in data transmission. A physical cable can generally accommodate several logical connections.

  For the FBs to open communication by means of Industrial Ethernet, the following connection oriented protocols are supported:

  - TCP native according to RFC 793 (connection types B#16#01 and B#16#11)
  - ISO on TCP according to RFC 1006 (connection type B#16#12)
- Connectionless protocols:

  These operate without a connection. There is also no establishing or terminating a connection to remote partner. Connectionless protocols transfer the data without acknowlegement and thus unsecured to the remote partner.
  The following connectionless protocol is supported at the FBs for open communication via Industrial Ethernet:

  - UDP according to RFC 768 (connection type B#16#13)

How to use open IE communication

To allow data to be exchanged with other communication partners, STEP 7 provides the following FBs and UDTs under "Communication Blocks" in the "Standard Library":

- Connection oriented protocols: TCP-native, ISO-on-TCP
  - FB 63 "TSEND" for sending data
  - FB 64 "TRCV" for receiving data
  - FB 65 "TCON", for connecting
  - FB 66 "TDISCON", for disconnecting
  - UDT 65 "TCON_PAR" with the data structure for the configuration of the connection
- Connectionless protocol: UDP
  - FB 67 "TUSEND" for sending data
  - FB 68 "TURCV" for receiving data
  - FB 65 "TCON" for establishing the local communication access point
  - FB 66 "TDISCON" for resolving the local communication access point
  - UDT 65 "TCON_PAR" with the data structure for configuring the local communication access point
  - UDT 66 "TCON_ADR" with the data structure of the address parameters of the remote partner

Data blocks for the configuration of the connection

- Data blocks for configuring TCP native and ISO-on-TCP connections.

  To configure your connection, you need to create a DB that contains the data structure of UDT 65 "TCON_PAR." This data structure contains all parameters you need to establish the connection. You need to create such a data structure for each connection, and you can also organize it in a global DB.

  Connection parameter CONNECT of FB 65 "TCON" reports the address of the corresponding connection description to the user program (for example, P#DB100.DBX0.0 byte 64).

- Data blocks for the configuration the local UDP communication access point

  To assign parameters for the local communication access point, create a DB containing the data structure from the UDT 65 "TCON_PAR" This data structure contains the required parameters you need to establish the connection between the user program and the communication level of the operating system

  The CONNECT parameter of the FB 65 "TCON" contains a reference to the address of the corresponding connection description (e.g. P#DB100.DBX0.0 Byte 64).

Note

Setting up the connection description (UDT 65)

The interface to be used for for communication (for example B#16#03: Communication via the integrated IE interface for the CPU 319-3 PN/DP) has to be entered in the UDT 65 "TCON_PAR" in the parameter "local_device_id".

Establishing a connection for communication

- Use with TCP native and ISO on TOP

  Both communication partners call FB 65 "TCON" to establish the connection. In your connection configuration, you define which communication partner activates the connection, and which communication partner responds to the request with a passive connection. To determine the number of possible connections, refer to your CPU's technical specifications.

  The CPU automatically monitors and holds the active connection.

  If the connection is broken, for example by line interruption or by the remote communication partner, the active partner tries to reestablish the connection. You do not have to call FB 65 "TCON" again.

  FB 66 "TDISCON" disconnects the CPU from a communication partner, as does STOP mode. To reestablish the connection to have to call FB65 "TCON" again.

- Use with UDP

  Both communication partners call FB 65 "TCON" to set up their local communication access point. This establishes a connection between the user program and operating system's communication level No connection is established to the remote partner.

  The local access point is used to send and receive UDP telegrams.

Disconnecting

- Use with TCP native and ISO on TCP

  FB 66 "TDISCON" disconnects the communication connection between CPU and communication partner.

- Use with UDP

  FB 66 "TDISCON" disconnects the local communication access point, i.e., the connection between user program and communication level of operating system is interrupted.

Options for interrupting the communication connection

Events causing interruptions of communication:

- You program the cancellation of connections at FB 66 "TDISCON."
- The CPU goes from RUN to STOP.
- At POWER OFF / POWER ON

Reference

For detailed information on the blocks described earlier, refer to the *STEP 7 Online Help.*

3.2.10.5 SNMP communication service

Availability

The SNMP communication service is available for CPUs with integrated PROFINET interface and Firmware 2.3.0 or higher.

Properties

SNMP (Simple Network Management Protocol)) is a standard protocol for TCP/IP networks.

Reference

For further information on the SNMP communication service and diagnostics with SNMP, refer to the *PROFINET System Description.*

3.3 S7 connections

3.3.1 S7 connection as communication path

An S7 connection is established when S7 modules communicate with one another. This S7 connection is the communication path.

Note

Global data communication, point-to-point connection, no S7 connections are required for communication via PROFIBUS DP, PROFINET CBA, PROFINET IO, TCP/IP, ISO on TCP, UDP and SNMP

Every communication link requires S7 connection resources on the CPU for the entire duration of this connection.

Thus, every S7 CPU provides a specific number of S7 connection resources. These are used by various communication services (PG/OP communication, S7 communication or S7 basic communication).

Connection points

An S7 connection between modules with communication capability is established between connection points. The S7 connection always has two connection points: The active and passive connection points:

- The active connection point is assigned to the module that establishes the S7 connection.
- The passive connection point is assigned to the module that accepts the S7 connection.

Any module that is capable of communication can thus act as an S7 connection point. At the connection point, the established communication link always uses one S7 connection of the module concerned.

Transition point

If you use the routing functionality, the S7 connection between two modules capable of communication is established across a number of subnets. These subnets are interconnected via a network transition. The module that implements this network transition is known as a router. The router is thus the point through which an S7 connection passes.

Any CPU with a DP or PN interface can be the router for an S7 connection. You can establish a certain maximum number of routing connections. This does not limit the data volume of the S7 connections.

See also

Connection resources for routing (Page 3-32)

3.3.2 Assignment of S7 connections

There are several ways to allocate S7 connections on a communication-capable module:

- Reservation during configuration
- Assigning connections in the program
- Allocating connections during commissioning, testing and diagnostics routines
- Allocating connection resources to HMI services

Reservation during configuration

One connection resource each is automatically reserved on the CPU for PG and OP communication. Whenever you need more connection resources (for example, when connecting several OPs), configure this increase in the CPU properties dialog box in STEP 7.

Connections must also be configured (using NetPro) for the use of S7 communication. For this purpose, connection resources have to be available, which are not allocated to PG/OP or other connections. The required S7 connections are then permanently allocated for S7 communication when the configuration is uploaded to the CPU.

Assigning connections in the program

In S7 basic communication, and in open Industrial Ethernet communication with TCP/IP, the user program establishes the connection. The CPU operating system initiates the connection. S7 basic communication uses the corresponding S7 connections. The open IE communication does not use any S7 connections. The maximum number of eight connections also applies to this type of communication.

Using connections for commissioning, testing and diagnostics

An active online function on the engineering station (PG/PC with STEP 7) occupies S7 connections for PG communication:

- An S7 connection resource for PG communication which was reserved in your CPU hardware configuration is assigned to the engineering station, that is, it only needs to be allocated.
- If all reserved S7 connection resources for PG communication are allocated, the operating system automatically assigns a free S7 connection resource which has not yet been reserved. If no more connection resources are available, the engineering station cannot go online to the CPU.

Allocating connection resources to HMI services

An online function on the HMI station (OP/TP/... with *WinCC*) is used for assigning S7 connection resources for the OP communication:

- An S7 connection resource for OP communication you have reserved in your CPU hardware configuration is therefore assigned to the OCM station engineering station, that is, it only needs to be allocated.
- If all reserved S7 connection resources for OP communication are allocated, the operating system automatically assigns a free S7 connection resource which has not yet been reserved. If no more connection resources are available, the OCM station cannot go online to the CPU.

Time sequence for allocation of S7 connection resources

When you program your project in STEP 7, the system generates parameter assignment blocks which are read by the modules in the startup phase. This allows the module's operating system to reserve or allocate the relevant S7 connection resources. That is, for instance, OPs cannot access a reserved S7 connection resource for PG communication. The CPU's S7 connection resources which were not reserved can be used freely. These S7 connection resources are allocated in the order they are requested.

Example

If there is only one free S7 connection left on the CPU, you can still connect a PG to the bus. The PG can then communicate with the CPU. The S7 connection is only used, however, when the PG is communicating with the CPU. If you connect an OP to the bus while the PG is not communicating, the OP can establish a connection to the CPU. Since an OP maintains its communication link at all times, in contrast to the PG, you cannot subsequently establish another connection via the PG.

See also

Open communication via Industrial Ethernet (Page 3-24)

3.3.3 Distribution and availability of S7 connection resources

Distribution of connection resources

Table 3-10 Distribution of connections

Communication service	Distribution
PG communication OP communication S7 basic communication	In order to avoid allocation of connection resources being dependent only on the chronological sequence in which various communication services are requested, connection resources can be reserved for these services. For PG and OP communication respectively, at least one connection resource is reserved by default. In the table below, and in the technical data of the CPUs, you can find the configurable S7 connection resources and the default configuration for each CPU. You "redistribute“ connection resources by setting the relevant CPU parameters in STEP 7.
S7 communication Other communication resources (e.g. via CP 343-1, with a data length of > 240 bytes)	Available connection resources that are not specially reserved for a service (PG/OP communication , S7 basis communication) are used for this.
Routing PG functions (only for CPUs with DP/PN interface)	The CPUs provide a certain number of connection resources for routing. These connections are available in addition to the connection resources. The subsection below shows the number of connection resources.
Global data communication Point-to-point communication	This communication service requires no S7 connection resources.
PROFIBUS DP	This communication service requires no S7 connection resources.
PROFINET CBA	This communication service requires no S7 connection resources.
PROFINET IO	This communication service requires no S7 connection resources.
Open communication by means of TCP/IP	This communication service requires no S7 connection resources.
Open communication by means of ISO on TCP	Independently of the S7 connections, a total of 8 own resources are available for connections or local access points (UDP) for TCP/IP, ISO on TCP, UDP.
Open communication by means of UDP	
SNMP	This communication service requires no S7 connection resources.

Availability of connection resources

Table 3-11 Availability of connection resources

CPU	Total number connection resources	Reserved for			Free S7 connections
		PG communication	OP communication	S7 basic communication	
312C	6	1 to 5, default 1	1 to 5, default 1	0 to 2, default 2	Displays all non-reserved S7 connection resources as free connection resources.
313C 313C-2 PtP 313C-2 DP	8	1 to 7, default 1	1 to 7, default 1	0 to 4, default 4	
314C-2 PtP 314C-2 DP	12	1 to 11, default 1	1 to 11, default 1	0 to 8, default 8	
312	6	1 to 5, default 1	1 to 5, default 1	0 to 2, default 2	
314	12	1 to 11, default 1	1 to 11, default 1	0 to 8, default 8	
315-2 DP 315-2 PN/DP	16	1 to 15, default 1	1 to 15, default 1	0 to 12, default 12	
317-2 DP 317-2 PN/DP	32	1 to 31, default 1	1 to 31, default 1	0 to 30, default 0	
319-3 PN/DP	32	1 to 31, default 1	1 to 31, default 1	0 to 30, default 0	

Note

When using a CPU 315-2 PN/DP, you can configure up to 14 connection resources for S7 communication in NetPro: These connections are then reserved. For CPU 317-2 PN/DP and CPU 319-3 PN/DP, you can configure a maximum of 16 coonnection resources for S7 communication in NetPro.

3.3.4 Connection resources for routing

Number of connection resources for routing

The CPUs with DP interface provide a different number of connection resources for the routing function:

Table 3-12 Number of routing connection resources (for DP/PN CPUs)

CPU	As of firmware version	Number of connections for routing
31xC, CPU 31x	2.0.0	Max. 4
317-2 DP	2.1.0	Max. 8
31x-2 PN/DP	2.2.0	Interface X1 configured as: • MPI:Max. 10 • DP master: Max. 24 • DP slave (active): Max. 14 Interface X2 configured as: • PROFINET: Max. 24
319-3 PN/DP	2.4.0	Interface X1 configured as: • MPI: Max. 10 • DP master: Max. 24 • DP slave (active): Max. 14 Interface X2 configured as: • DP master: Max. 24 • DP slave (active): Max. 14 Interface X3 configured as: PROFINET: Max. 48

Example of a CPU 314C-2 DP

The CPU 314C-2 DP provides 12 connection resources (refer to Table 3-11):

- Reserve two connection resources for PG communication.
- Reserve three connection resources for OP communication.
- Reserve one connection resource for S7-based communication.

This leaves six connection resources available for other communication service, e.g. S7 communication, OP communication, etc.

In addition 4 routing connections via the CPU are possible.

Example for a CPU 317-2 PN/DP / CPU 319-3 PN/DP

The CPU 317-2 PN/DP and CPU 319-3 PN/DP provide you with 32 connection resources (refer to Table 3-11):

- Reserve four connection resources for PG communication.
- Reserve six connection resources for OP communication.
- Reserve two connection resources for S7-based communication.
- In NetPro you configure eight S7 connection resources for S7 communication via the integrated PROFINET interface

This leaves 12 S7 connections available for arbitrary communication services, e.g. S7 communication, OP communication, etc.

However, only a maximum of 16 connection ressources for S7 communication at the integrated PN interface can be configured in NetPro.

In addition, there are another 24 routing connections available for the CPU 317-2 PN/DP, and another 48 routing connections for the CPU 319-3 PN/DP, which do not affect the aforementioned S7 connections.

However, take the interface-specific maximum numbers into account (refer to Table 3-12).

3.4 DPV1

New automation and process engineering tasks require the range of functions performed by the existing DP protocol to be extended. In addition to cyclical communication functions, acyclical access to non-S7 field devices is another important requirement of our customers, and was implemented in the standard EN 50170. In the past, acyclical access was only possible with S7 slaves. The distributed I/O standard EN 50170 has been further developed. All the changes concerning new DPV1 functions are included in IEC 61158/ EN 50170, volume 2, PROFIBUS.

Definition DPV1

The term DPV1 is defined as a functional extension of the acyclical services (to include new interrupts, for example) provided by the DP protocol.

Availability

All CPUs with DP interface(s) and serving as DP masters feature the enhanced DPV1 functionality.

Note

If you want to use the CPU as an intelligent slave, remember that it does not have DPV1 functionality.

Requirement for using the DPV1 functionality with DP slaves

For DPV1 slaves from other vendors, you will need a GSD file conforming to EN 50170, revision 3 or later.

Extended functions of DPV1

- Use of any DPV1 slaves from external vendors (in addition to the existing DPV0 and S7 slaves, of course).
- Selective handling of DPV1-specific interrupt events by new interrupt blocks.
- Reading/writing SFBs that conform to standards to the data record (although this can only be used for centralized modules).
- User-friendly SFB for reading diagnostics.

Interrupt blocks with DPV1 functionality

Table 3-13 Interrupt blocks with DPV1 functionality

OB	Functionality
OB 40	Process interrupt
OB 55	Status interrupt
OB 56	Update interrupt
OB 57	Vendor-specific interrupt
OB 82	Diagnostic interrupt

Note

You can now also use organizational blocks OB40 and OB82 for DPV1 interrupts.

System blocks with DPV1 functionality

Table 3-14 System function blocks with DPV1 functionality

SFB	Functionality
SFB 52	Read data record from DP slave/IO device or centralized module
SFB 53	Write data record to DP slave/IO device or centralized module
SFB 54	Read additional alarm information from a DP slave/IO device or a centralized module in the relevant OB
SFB 75	Set any interrupts for intelligent slaves

Note

You can also use SFB 52 to SFB 54 for centralized I/O modules. SFBs 52 to 54 can also be used for PN IO.

Reference

For further information on the blocks mentioned earlier, refer to the reference manual *System Software for S7-300/400: System and Standard Software*, or directly to the *STEP 7Online Help*.

See also

PROFIBUS DP (Page 3-2)

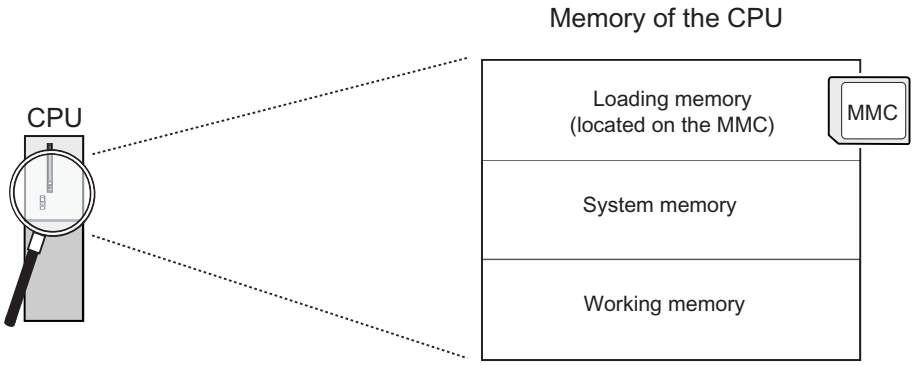
Memory concept

4

4.1 Memory areas and retentivity

4.1.1 CPU memory areas

The three memory areas of your CPU:



Load memory

The load memory is located on the SIMATIC Micro Memory Card (MMC). The size of the load memory corresponds exactly to the size of the SIMATIC Micro Memory Card. It is used to store code blocks, data blocks and system data (configuration, connections, module parameters, etc.). Blocks that are identified as non runtime-related are stored exclusively in load memory. You can also store all the configuration data for your project on the SIMATIC Micro Memory Card.

Note

User programs can only be downloaded and thus the CPU can only be used if the SIMATIC Micro Memory Card is inserted in the CPU.

System memory

The RAM system memory is integrated in the CPU and cannot be expanded.

It contains

- the address areas for address area memory bits, timers and counters
- the process image of the I/Os
- local data

RAM

The RAM is integrated in the CPU and cannot be extended. It is used to run the code and process user program data. Programs only run in RAM and system memory.

Table 4-1 Retentivity of the RAM

All CPUs except: CPU 317, CPU 319	RAM is always retentive.	
317	256 KB of RAM can be used for retentive data modules.	
319	700 KB of RAM can be used for retentive data modules.	

4.1.2 Retentivity of load memory, system memory and RAM

Your CPU is equipped with a service-free retentive memory, i.e. its operation does not require a buffer battery. Data is kept in retentive memory across POWER OFF and restart (warm start).

Retentive data in load memory

Your program in load memory is always retentive: It is stored on the SIMATIC Micro Memory Card, where it is protected against power failure or CPU memory restart

Retentive data in system memory

In your configuration (Properties of CPU, Retentivity tab), specify which part of memory bits, timers and counters should be kept retentive and which of them are to be initialized with "0" on restart (warm restart).

The diagnostic buffer, MPI address (and transmission rate) and operating hour counter data are generally written to the retentive memory area on the CPU. Retentivity of the MPI address and baud rate ensures that your CPU can continue to communicate, even after a power loss, memory reset or loss of communication parameters (e.g. due to removal of the SIMATIC Micro Memory Card or deletion of communication parameters).

Retentive data in RAM

Therefore, the contents of retentive DBs are always retentive at restart and POWER ON/OFF.

CPUs V2.1.0 or higher also support volatile DBs (the volatile DBs are initialized at restart of POWER OFF-ON with their initial values from load memory.)

See also

Properties of the SIMATIC Micro Memory Card (MMC) (Page 4-8)

4.1.3 Retentivity of memory objects

Retentive behavior of memory objects

The table below shows the retentive behavior of memory objects during specific operating state transitions.

Table 4-2 Retentivity behavior of memory objects (applies to all CPUs with DP/MPI-SS)

Memory object	Operating state transition		
	POWER ON / POWER OFF	STOP → RUN	CPU memory reset
User program/data (load memory)	X	X	X
• Retentive behavior of DBs for CPUs with firmware < V2.1.0	X	X	–
• Retentive behavior of DBs for CPUs with firmware >= V2.1.0	Can be set in the properties of the DBs in STEP 7 V5.2 + SP1 or higher.		–
Flag bits, timers and counters configured as retentive data	X	X	–
Diagnostics buffers, operating hour counters	X	X	X
MPI address, transmission rate (or also DP address, transmission rate of the MPI/DP interface of CPU 315-2 PN/DP and CPU 317 and CPU 319, if these are configured as DP nodes).	X	X	X

x = retentive; – = not retentive

Retentive behavior of a DB for CPUs with firmware < V2.1.0

For these CPUs, the contents of the DBs are always retentive at POWER ON/OFF or STOP-RUN.

Retentive behavior of a DB for CPUs with firmware >= V2.1.0

For these CPUs you can specify in STEP 7 (beginning with version 5.2 + SP 1), or at SFC 82 CREA_DBL (parameter ATTRIB -> NON_RETAIN bit), whether a DB at POWER ON/OFF or RUN-STOP

- keeps the actual values (retentive DB), or
- accepts the initial values from load memory (non-retentive DB)

Table 4-3 Retentive behavior of DBs for CPUs with firmware >= V2.1.0

At POWER ON/OFF or restart (warm start) of the CPU, the DB should	
receive the initial values (non-retentive DB)	**retain the actual values (retentive DB)**
Reason: At POWER ON/OFF and restart (STOP-RUN) of the CPU, the actual values of the DB are non-retentive. The DB receives the start values from load memory.	Reason: At POWER OFF/ON and restart (STOP-RUN) of the CPU, the actual values of the DB are retained.
Requirement in STEP 7: • The "Non-retain" check box must be set in the block properties of the DB, or • a non-retentive DB was generated with SFC 82 "CREA_DBL" and the corresponding block attribute (ATTRIB -> NON_RETAIN bit.)	Requirement in STEP 7: • The "Non-retain" check box must be reset in the block properties of the DB or • a retentive DB was generated with SFC 82.

Note

Note:

- Only 256 KB of RAM can be used for retentive DBs on a CPU 317.
- Only 700 KB of RAM can be used for retentive DBs on a CPU 319.

The remainder of the RAM is used by code blocks and non-retentive data blocks.

4.1.4 Address areas of system memory

The system memory of the S7 CPUs is organized in address areas (refer to the table below). In a corresponding operation of your user program, you address data directly in the relevant address area.

Address areas of system memory

Table 4-4 Address areas of system memory

Address areas	Description
Process image of inputs	At every start of an OB1 cycle, the CPU reads the values at the input of the input modules and saves them the process image of inputs.
Process image of outputs	During its cycle, the program calculates the values for the outputs and writes these to the process image of outputs. At the end of the OB1 cycle, the CPU writes the calculated output values to the output modules.
Flag bits	This area provides memory for saving the intermediate results of a program calculation.
Timers	Timers are available in this area.
Counters	Counters are available in this area.
Local data	Temporary data in a code block (OB, FB, FC) is saved to this memory area while the block is being edited.
Data blocks	See *Recipes and measurement value logs*

Reference

The address areas of your CPU are listed in the *Instruction list for CPUs 31xC and 31x*.

I/O process image

When the user program addresses the input (I) and output (O) address areas, it does not query the signal states of digital signal modules. Instead, it rather accesses a memory area in CPU system memory. This particular memory area is the process image.

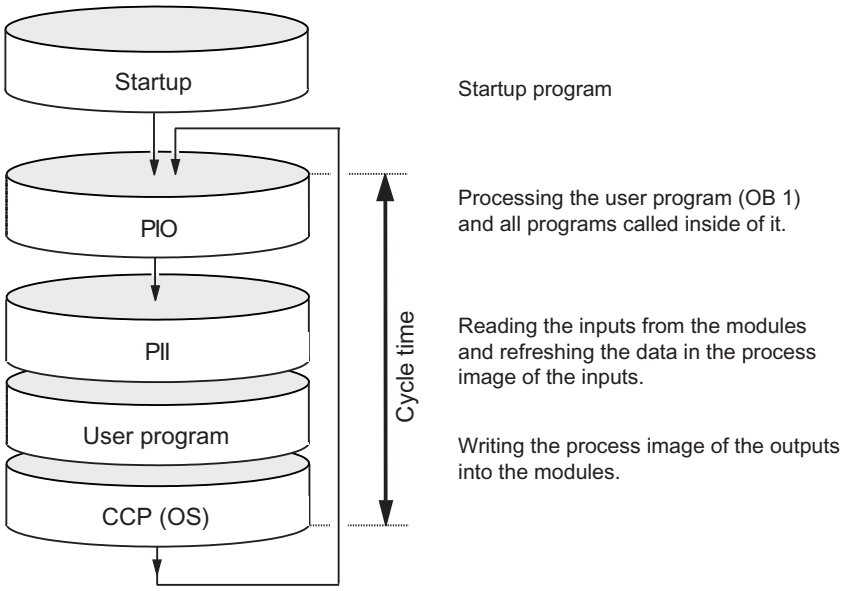
The process image is organized in two sections: The process image of inputs, and the process image of outputs.

Advantages of the process image

Process image access, compared to direct I/O access, offers the advantage that a consistent image of process signals is made available to the CPU during cyclic program execution. When the signal status at an input module changes during program execution, the signal status in the process image is maintained until the image is updated in the next cycle. Moreover, since the process image is stored in CPU system memory, access is significantly faster than direct access to the signal modules.

Process image update

The operating system updates the process image periodically. The figure below shows the sequence of this operation within a cycle.



Configurable process image with CPUs that have FW V2.3.0 or higher

In STEP 7, you can define a user-specific size of the I/O process images between 0 to 2048 for the CPUs, FW V2.3.0 or higher.

Note the information below:

Note

Currently, the dynamic setting of the process image only affects its update at the scan cycle control point. That is, the process image of inputs is only updated up to the set PII size with the corresponding values of the peripheral input modules existing within this address area, or the values of the process image of outputs up to the set PIO size are written to the peripheral output modules existing within this address area.

This set size of the process image is ignored with respect to STEP 7 commands used to access the process image (for example U I100.0, L EW200, = Q20.0, T AD150, or corresponding indirect addressing commands also). However, up to the maximum size of the process image (that is, up to I/O byte 2047), these commands do not return any synchronous access errors, but rather access the permanently available internal memory area of the process image.
The same applies to the use of actual parameters of block calls from the I/O area (area of the process image).

Particularly if these process image limits were changed, you should check to which extent your user program accesses the process image in the area between the set and the maximum process image size. If access to this area continues, the user program may not detect changes at the inputs of the I/O module, or actually fails to write the data of outputs to the output module, without the system generating an error message.
You should also note that certain CPs may only be addressed outside of the process image.

Local data

Local data store:

- the temporary variables of code blocks
- the start information of the OBs
- transfer parameters
- intermediate results

Temporary Variables

When you create blocks, you can declare temporary variables (TEMP) which are only available during block execution and then overwritten again. These local data have fixed length in each OB. Local data must be initialized prior to the first read access. Each OB also requires 20 bytes of local data for its start information. Local data access is faster compared to access to data in DBs.

The CPU is equipped with memory for storing temporary variables (local data) of currently executed blocks. The size of this memory area depends on the CPU. It is distributed in partitions of equal size to the priority classes. Each priority class has its own local data area.

Caution

All temporary variables (TEMP) of an OB and its nested blocks are stored in local data. When using complex nesting levels for block processing, you may cause an overflow in the local data area.
The CPUs will change to STOP mode if you exceed the permissible length of local data for a priority class.
Make allowances for local data space required for synchronous error OBs. This is assigned to the respective triggering priority class.

See also

Retentivity of load memory, system memory and RAM (Page 4-2)

4.1.5 Properties of the SIMATIC Micro Memory Card (MMC)

The SIMATIC Micro Memory Card (MMC) as memory module for the CPU

The memory module used on your CPU is a SIMATIC Micro Memory Card. You can use MMCs as load memory or as a portable storage medium.

Note

The CPU requires the SIMATIC Micro Memory Card for operation.

The following data are stored on the SIMATIC Micro Memory Card.

- User programs (all blocks)
- Archives and recipes
- Configuration data (STEP 7 projects)
- Data for operating system update and backup

Note

You can either store user and configuration data or the operating system on the SIMATIC Micro Memory Card.

Properties of the SIMATIC Micro Memory Card (MMC)

The SIMATIC Micro Memory Card ensures maintenance-free and retentive operation of these CPUs.

Caution

Data on a SIMATIC Micro Memory Card can be corrupted if you remove the card while it is being accessed by a write operation. In this case, you may have to delete the SIMATIC Micro Memory Card on your PG, or format the card in the CPU. Never remove a SIMATIC Micro Memory Card in RUN mode. Always remove it when power is off, or when the CPU is in STOP state, and when the PG is not writing to the card. When the CPU is in STOP mode and you cannot not determine whether or not a PG is writing to the card (e.g. load/delete block), disconnect the communication lines.

SIMATIC Micro Memory Card (MMC) copy protection

Your SIMATIC Micro Memory Card has an internal serial number that implements an MMC copy protection. You can read this serial number from the SSL partial list $011C_H$ index 8 using SFC 51 "RDSYSST." If the reference and actual serial number of your SIMATIC Micro Memory Card are not the same, program a STOP command in a know-how-protected module, for example.

Reference

Further information

- on *SZL parts list* refer to the *Instruction list* or the *System and Standard functions* manual.
- on resetting the CPU, refer to the *Operating instructions CPU 31xC and CPU31x, Commissioning, Commissioning Modules, CPU Memory Reset by means of Mode Selector Switch*

Useful life of a SIMATIC Micro Memory Card (MMC)

The life of an SIMATIC Micro Memory Card depends mainly on the following factors:

1. The number of delete or programming operations,
2. External influences such as ambient temperature.

At ambient temperatures up to 60 °C, a maximum of 1000,000 delete/write operations can be performed on a SIMATIC Micro Memory Card.

Caution

To prevent loss of data, always make sure that you do not exceed the maximum number of delete/write operations.

See also

Operating and display elements: CPU 31xC (Page 2-1)

Operating and display elements: CPU 312, 314, 315-2 DP: (Page 2-5)

Operating and display elements: CPU 317-2 DP (Page 2-7)

Operating and display elements: CPU 31x-2 PN/DP (Page 2-9)

Operating and display elements: CPU 319-3 PN/DP (Page 2-11)

4.2 Memory functions

4.2.1 General: Memory functions

Memory functions

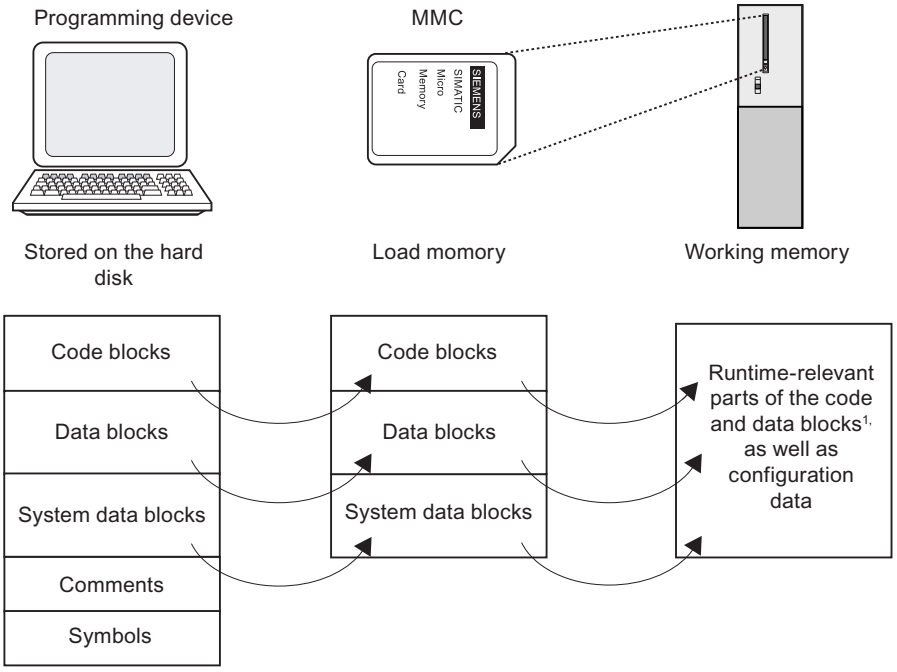
Memory functions are used to generate, modify or delete entire user programs or specific blocks. You can also ensure that your project data are retained by archiving these. If you created a new user program, use a PG/PC to download the complete program to the SIMATIC Micro Memory Card.

4.2.2 Loading user program from SIMATIC Micro Memory Card (MMC) to the CPU

User program download

The entire user program data are downloaded from your PG/PC to the SIMATIC Micro Memory Card (MMC). The previous content of the MMC is deleted in the process. Blocks use the load memory area as specified under "Load memory requirements" in "General block properties".

The figure shows the load and work memory of the CPU



1: If not all of the work memory area is retentive, the retentive area is indicated in STEP 7 module status as retentive memory (same as on CPU 317). You cannot run the program until all the blocks are downloaded.

Note

This function is only permitted when the CPU is in STOP mode. Load memory is cleared if the load operation could not be completed due to power loss or illegal block data.

4.2.3 Handling with modules

4.2.3.1 Download of new blocks or delta downloads

There are two ways to download additional user blocks or download deltas:

- Download of blocks: You already created a user program and downloaded it to the CPU via the SIMATIC Micro Memory Card. You then want to add new blocks to the user program. In this case you do not need to reload the entire user program to the MCC. Instead you only need to download the new blocks to the SIMATIC Micro Memory Card (this reduces the download times for highly complex programs.)
- Delta download: In this case, you only download the deltas in the blocks of your user program. In the next step, perform a delta download of the user program, or only of the changed blocks to the SIMATIC Micro Memory Card, using the PG/PC.

Warning

The delta down of block / user programs overwrites all data stored under the same name on the SIMATIC Micro Memory Card.

The data of dynamic blocks are transferred to RAM and activated after the block is downloaded.

4.2.3.2 Uploading blocks

Uploading blocks

Unlike download operations, an upload operation is the transfer of specific blocks or a complete user program from the CPU to the PG/PC. The block content is here identical with that of the last download to the CPU. Dynamic DBs form the exception, because their actual values are transferred. An upload of blocks or of the user program from the CPU in STEP 7 does not influence CPU memory.

4.2.3.3 Deleting blocks

Deleting blocks

When you delete a block, it is deleted from load memory. In STEP 7, you can also delete blocks with the user program (DBs also with SFC 23 "DEL_DB"). RAM used by this block is released.

4.2.3.4 Compressing blocks

Compressing blocks

When data are compressed, gaps which have developed between memory objects in load memory/RAM as a result of load/delete operations will be eliminated. This releases free memory in a continuous block. Data compression is possible when the CPU is in RUN or in STOP.

4.2.3.5 Promming (RAM to ROM)

Promming (RAM to ROM)

When writing the RAM content to ROM, the actual values of the DBs are transferred from RAM to load memory to form the start values for the DBs.

Note

This function is only permitted when the CPU is in STOP mode. Load memory is cleared if the function could not be completed due to power loss.

4.2.4 CPU memory reset and restart

CPU memory reset

After the insertion/removal of a Micro Memory Card, a CPU memory reset restores defined conditions for CPU restart (warm start). A CPU memory reset rebuilds the CPU's memory management. Blocks in load memory are retained. All dynamic runtime blocks are transferred once again from load memory to RAM, in particular to initialize the data blocks in RAM (restore initial values).

Restart (warm start)

- All retentive DBs retain their actual value (non-retentive DBs are also supported by CPUs with Firmware >= V2.1.0. Non-retentive DBs receive their initial values).
- The values of all retentive M, C, T are retained.
- All non-retentive user data are initialized:
  - M, C, T, I, O with "0"
- All run levels are initialized.
- The process images are deleted.

Reference

Also refer to *CPU memory reset by means mode selector switch* in the section *Commissioning* in the *CPU 31xC and CPU 31x Operating Instructions*.

4.2.5 Recipes

Introduction

A recipe represents a collection of user data. You can implement a simple recipe concept using static DBs. In this case, the recipes should have the same structure (length). One DB should exist per recipe.

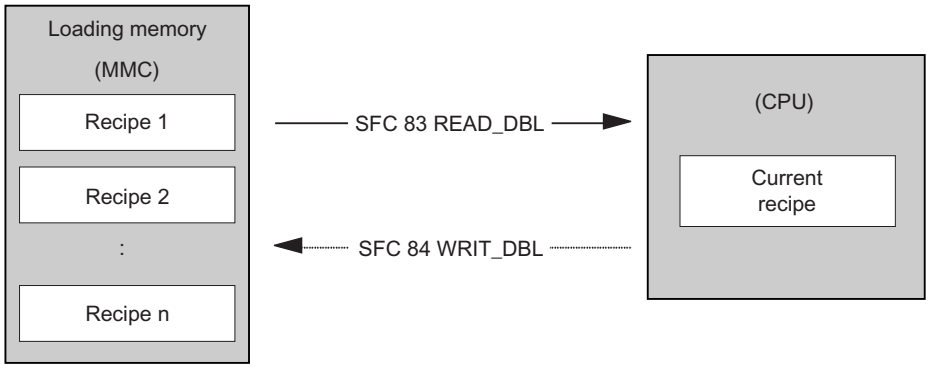
Processing sequence

Recipe is written to load memory:

- The various data records of recipes are created as static DBs in STEP 7 and then downloaded to the CPU. Therefore, recipes only use load memory, rather than RAM.

Working with recipe data:

- SFC83 "READ_DBL" is called in the user program to copy the data record of a current recipe from the DB in load memory to a static DB that is located in work memory. As a result, the RAM only has to accommodate the data of one record. The user program can now access data of the current recipe. The figure below shows how to handle recipe data:



Saving a modified recipe:

- The data of new or modified recipe data records generated during program execution can be written to load memory. To do this, call SFC 84 "WRIT_DBL" in the user program. These data written to load memory are portable and also retentive on memory reset. You can backup modified records (recipes) by uploading and saving these in a single block to the PG/PC.

Note

Active system functions SFC82 to 84 (active access to the SIMATIC Micro Memory Card) have a distinct influence on PG functions (for example, block status, variable status, download block, upload, open.) This typically reduces performance (compared to passive system functions) by the factor 10.

Note

As a precaution against loss of data, always make sure that you do not exceed the maximum number of delete/write operations. Also refer to the SIMATIC Micro Memory Card (MMC) section in the "Structure and Communication Connections of a CPU" chapter.

Caution

Data on a SIMATIC Micro Memory Card can be corrupted if you remove the card while it is being accessed by a write operation. In this case, you may have to delete the SIMATIC Micro Memory Card on your PG, or format the card in the CPU. Never remove a SIMATIC Micro Memory Card in RUN mode. Always remove it when power is off, or when the CPU is in STOP state, and when the PG is not writing to the card. When the CPU is in STOP mode and you cannot not determine whether or not a PG is writing to the card (e.g. load/delete block), disconnect the communication lines.

4.2.6 Measured value log files

Introduction

Measured values are generated when the CPU executes the user program. These values are to be logged and analyzed.

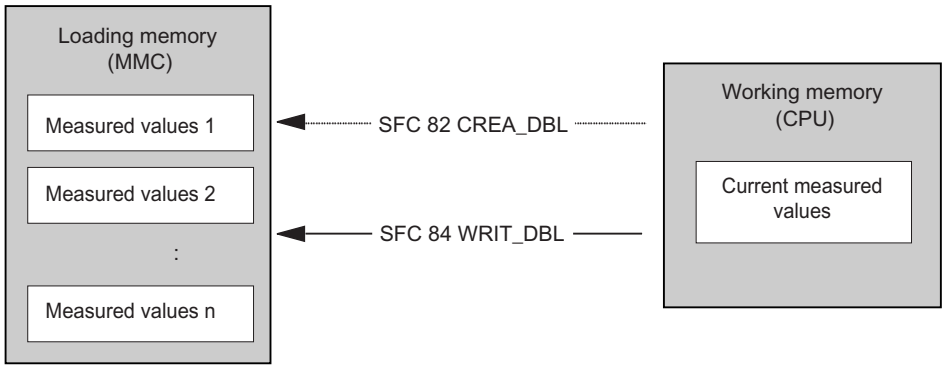
Processing sequence

Acquisition of measured values:

- The CPU writes all measured values to a DB (for alternating backup mode in several DBs) which is located in RAM.

Measured value logging:

- Before the data volume can exceed work memory capacity, you should call SFC 84 "WRIT_DBL" in the user program to swap measured values from the DB to load memory. The figure below shows how to handle measured value log files:



- You can call SFC 82 "CREA_DBL" in the user program to generate new (additional) static DBs in load memory which do not require RAM space.

Reference

For detailed information on SFC 82, refer to the *System Software for S7-300/400, System and Standard Functions* Reference Manual, or directly to the STEP 7 Online Help.

Note

SFC 82 is terminated and an error message is generated if a DB already exists under the same number in load memory and/or RAM.

The data written to load memory are portable and retentive on CPU memory reset.

Evaluation of measured values:

- Measured value DBs saved to load memory can be uploaded and evaluated by other communication partners (PG, PC, for example).

Note

Active system functions SFC82 to 84 (active access to the SIMATIC Micro Memory Card) have a distinct influence on PG functions (for example, block status, variable status, download block, upload, open.) This typically reduces performance (compared to passive system functions) by the factor 10.

Note

For CPUs with firmware V2.1.0 or higher, you can also generate non-retentive DBs using SFC 82 (parameter ATTRIB -> NON_RETAIN bit.)

Note

To prevent data losses, do not exceed this maximum of delete/write operations. For further information, refer to the Technical Data of the SIMATIC Micro Memory in the General Technical Data of your CPU.

Caution

Data on a SIMATIC Micro Memory Card can be corrupted if you remove the card while it is being accessed by a write operation. In this case, you may have to delete the SIMATIC Micro Memory Card on your PG, or format the card in the CPU. Never remove a SIMATIC Micro Memory Card in RUN mode. Always remove it when power is off, or when the CPU is in STOP state, and when the PG is not writing to the card. When the CPU is in STOP mode and you cannot not determine whether or not a PG is writing to the card (e.g. load/delete block), disconnect the communication lines.

4.2.7 Backup of project data to SIMATIC Micro Memory Card (MMC)

Function principle

Using the **Save project to Memory Card** and **Fetch project from Memory Card** functions, you can save all project data to a SIMATIC Micro Memory Card, and retrieve these at a later time. For this operation, the SIMATIC Micro Memory Card can be located in a CPU or in the MMC adapter of a PG or PC.

Project data are compressed before they are saved to a SIMATIC Micro Memory Card, and uncompressed when fetched.

Note

In addition to project data, you may also have to store your user data on the MMC. You should therefore first verify SIMATIC Micro Memory Card memory space.

A message warns you if the memory capacity on your SIMATIC Micro Memory Card is insufficient

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The volume of project data to be saved corresponds with the size of the project's archive file.

Note

For technical reasons, you can only transfer the entire contents (user program and project data) using the **Save project to memory card** action.

Cycle and reaction times

5

5.1 Overview

Overview

This section contains detailed information about the following topics:

- Cycle time
- Reaction time
- Interrupt response time
- Sample calculations

Reference: Cycle time

You can view the cycle time of your user program on the PG. For further information, refer to the *STEP 7 Online Help*, or to the *Configuring Hardware and Connections in STEP 7* Manual

Reference: Execution time

can be found in the *S7-300 Instruction List for CPUs 31xC and 31x*. This tabular list contains the execution times for all

- STEP 7 instructions the relevant CPU can execute,
- the SFCs / SFBs integrated in the CPUs,
- the IEC functions which can be called in STEP 7.

5.2 Cycle time

5.2.1 Overview

Introduction

This section explains what we mean by the term "cycle time", what it consists of, and how you can calculate it.

Meaning of the term cycle time

The cycle time represents the time that an operating system needs to execute a program, that is, one OB 1 cycle, including all program sections and system activities interrupting this cycle. This time is monitored.

Time slice model

Cyclic program processing, and therefore user program execution, is based on time shares. To clarify these processes, let us assume that every time share has a length of precisely 1 ms.

Process image

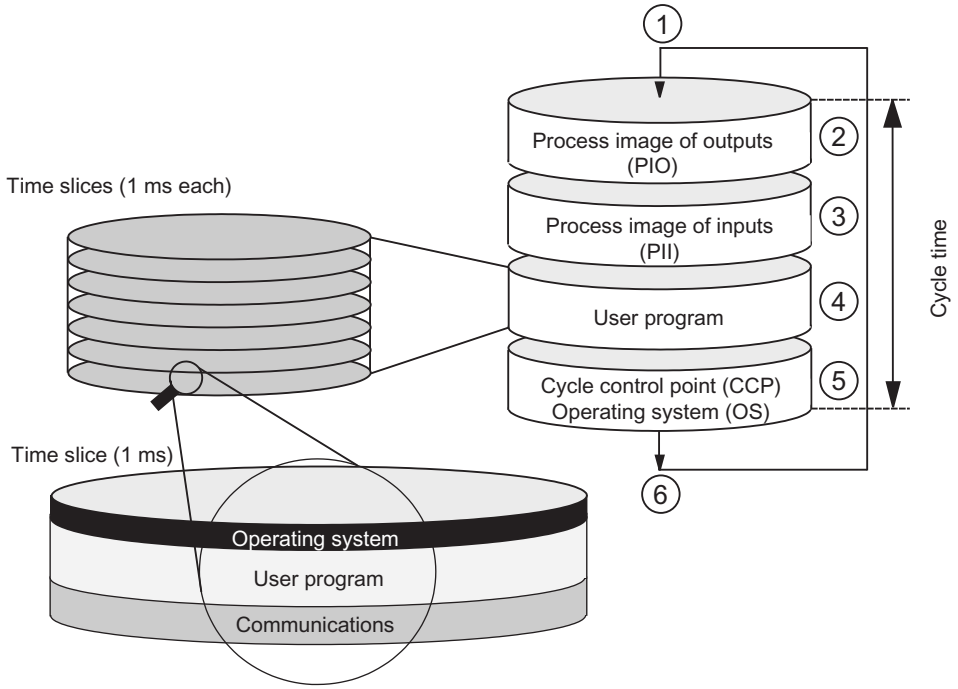
During cyclic program processing, the CPU requires a consistent image of the process signals. To ensure this, the process signals are read/written prior to program execution. Subsequently, the CPU does not address input (I) and output (Q) address areas directly at the signal modules, but rather accesses the system memory area containing the I/O process image.

Sequence of cyclic program processing

The table and figure below show the phases in cyclic program processing.

Table 5-1 Cyclic program processing

Step	Sequence
1	The operating system initiates cycle time monitoring.
2	The CPU copies the values of the process image of outputs to the output modules.
3	The CPU reads the status at the inputs of the input modules and then updates the process image of inputs.
4	The CPU processes the user program in time shares and executes program instructions.
5	At the end of a cycle, the operating system executes queued tasks, for example, loading and deleting blocks.
6	The CPU then returns to the start of the cycle, and restarts cycle time monitoring.



In contrast to S7-400 CPUs, the S7-300 CPUs data only allow data access from an OP / TP (monitor and modify functions) at the scan cycle check point (Data consistency, see the Technical Data). Processing of the user program is not interrupted by the monitor and modify functions.

Extending the cycle time

Always make allowances for the extension of the cycle time of a user program due to:

- Time-based interrupt processing
- Process interrupt processing
- Diagnostics and error processing
- Communication with PGs, Operator Panels (OPs) and connected CPs (for example, Ethernet, PROFIBUS DP)
- Testing and commissioning such as, e.g. status/controlling of variables or block status functions.
- Transfer and deletion of blocks, compressing user program memory
- Write/read access to the MMC, using SFC 82 to 84 in the user program
- Ethernet communication via integrated PROFINET interface
- PROFINET CBA communication by means of the PROFINET interface (system load, SFC call, updating on the cycle control point)
- PROFINET IO communication via PROFINET interface (system load)

5.2.2 Calculating the cycle time

Introduction

The cycle time is derived from the sum of the following influencing factors.

Process image update

The table below shows the time a CPU requires to update the process image (process image transfer time). The times specified might be prolonged as a result of interrupts or CPU communication. The process image transfer time is calculated as follows:

Table 5-2 Formula for calculating the process image (PI) transfer time

The transfer time of the process image is calculated as follows:	
Base load K	+ number of bytes in PI in module rack 0 x (A)
	+ number of bytes in PO in module rack 1 to 3 x (B)
	+ number of words in PO via DP x (D)
	+ number of words in PO via PROFINET x (P)
	= Transfer time for the process image

Table 5-3 CPU 31xC: Data for calculating the process image (PI) transfer time

Const.	Components	CPU 312C	CPU 313C	CPU 313C-2 DP	CPU 313C-2 PtP	CPU 314C-2 DP	CPU 314C-2 PtP
C	Base load	150 µs	100 µs	100 µs		100 µs	
A	Per byte in the rack 0	37 µs	35 µs	37 µs		37 µs	
B	per byte in module racks 1 to 3 *	-	43 µs	47 µs		47 µs	
D (DP only)	Per word in the DP area for the integrated DP interface	-	-	1 µs	-	1 µs	-

* + 60 µs per rack

Table 5-4 CPU 31x: Data for calculating the process image (PI) transfer time

Const.	Components	CPU 312	CPU 314	CPU 315	CPU 317	CPU 319
C	Base load	150 µs	100 µs	100 µs	50 µs	2 µs
A	Per byte in the rack 0	37 µs	35 µs	37 µs	15 µs	15 µs
B	per byte in module racks 1 to 3 *	-	43 µs*	47 µs*	25 µs*	22 µs**
D (DP only)	Per word in the DP area for the integrated DP interface	-	-	2,5 µs	2,5 µs	2,5 µs
P (PROFINET only)	per WORD in the PROFINET area for the integrated PROFINET interface	-	-	46 µs	46 µs	2,5 µs

* + 60 µs per rack
** + 21 µs per rack

Extending the user program processing time

In addition to actually working through the user program, your CPU's operating system also runs a number of processes in parallel
(such as timer management for the core operating system). These processes extend the processing time of the user program. The table below lists the multiplication factors required to calculate your user program processing time.

Table 5-5 Extending the user program processing time

CPU	Factor
312C	1,06
313C	1,10
313C-2DP	1,10
313C-PtP	1,06
314C-2DP	1,10
314C-2PtP	1,09
312	1,06
314	1,10
315	1,10
317	1,07
319	1,05

Operating system processing time at the scan cycle check point

The table below shows the operating system processing time at the scan cycle checkpoint of the CPUs. These times are calculated without taking into consideration times for:

- Testing and commissioning routines, e.g. status/controlling of variables or block status functions
- Transfer and deletion of blocks, compressing user program memory
- Communication
- Writing, reading of the SIMATIC Micro Memory Card with SFC 82 to 84

Table 5-6 Operating system processing time at the scan cycle check point

CPU	Cycle control at the scan cycle check point (CCP)
312C	500 µs
313C	500 µs
313C-2	500 µs
314C-2	500 µs
312	500 µs
314	500 µs
315	500 µs
317	150 µs
319	77 µs

Extension of the cycle time as a result of nested interrupts

Enabled interrupts also extend cycle time. Details are found in the table below.

Table 5-7 Extended cycle time due to nested interrupts

Interrupt type	Process interrupt	Diagnostic Interrupt	Time-of-day interrupt	Delay interrupt	Watchdog interrupt
312C	700 µs	700 µs	600 µs	400 µs	250 µs
313C	500 µs	600 µs	400 µs	300 µs	150 µs
313C-2	500 µs	600 µs	400 µs	300 µs	150 µs
314C-2	500 µs	600 µs	400 µs	300 µs	150 µs
312	700 µs	700 µs	600 µs	400 µs	250 µs
314	500 µs	600 µs	400 µs	300 µs	150 µs
315	500 µs	600 µs	400 µs	300 µs	150 µs
317	190 µs	240 µs	200 µs	150 µs	90 µs
319	72 µs	87 µs	39 µs	26 µs	10 µs

The program runtime at interrupt level must be added to this time extension.

Extension of the cycle time due to error

Table 5-8 Cycle time extension as a result of errors

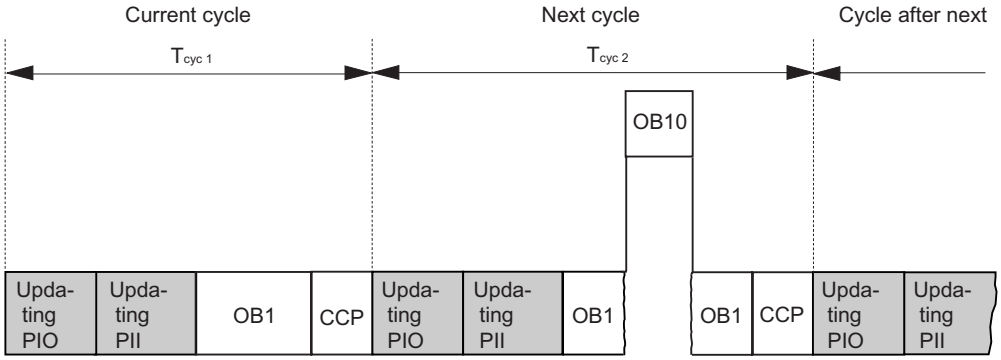
Type of error	Programming errors	I/O access errors
312C	600 µs	600 µs
313C	400 µs	400 µs
313C2	400 µs	400 µs
314C-2	400 µs	400 µs
312	600 µs	600 µs
314	400 µs	400 µs
315	400 µs	400 µs
317	100 µs	100 µs
319	19 µs	23 µs

The interrupt OB processing time must be added to this extended time. The times required for multiple nested interrupt/error OBs are added accordingly.

5.2.3 Different cycle times

Overview

The cycle time (T_{cyc}) length is not the same in every cycle. The figure below shows different cycle times T_{cyc1} and T_{cyc2}. T_{cyc2} is longer than T_{cyc1}, because the cyclically executed OB1 is interrupted by a time-of-day interrupt OB (here: OB 10).



Block processing times may fluctuate

Fluctuation of the block processing time (e.g. OB 1) may also be a factor causing cycle time fluctuation, due to:

- conditional instructions,
- conditional block calls,
- different program paths,
- loops etc.

Maximum cycle time

In *STEP 7* you can modify the default maximum cycle time. OB80 is called on when this time expires. In this block you can specify the CPUs response to this timeout error. The CPU switches to STOP mode if OB80 does not exist in its memory.

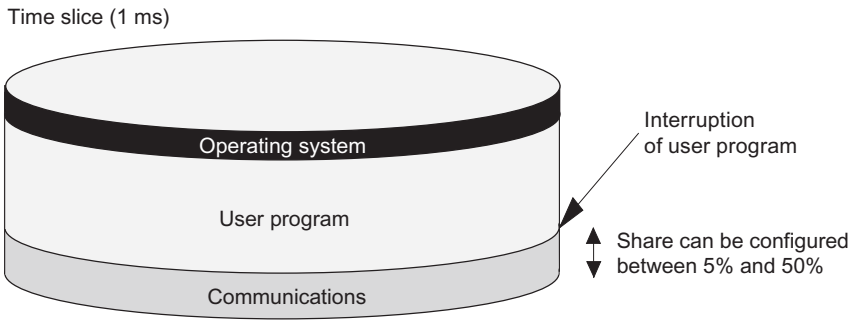
5.2.4 Communication load

Configured communication load for PG/OP communication, S7 communication and PROFINET CBA

The CPU operating system continuously provides a specified percentage of total CPU processing performance (time-sharing technology) for communication tasks. Processing performance not required for communication is made available to other processes. In HW Config, you can specify a communication load value between 5% and 50%. Default value is 20%.

You can use the following formula for calculating the cycle time extension factor:

100 / (100 – configured communication load in %)



Example: 20 % communication load

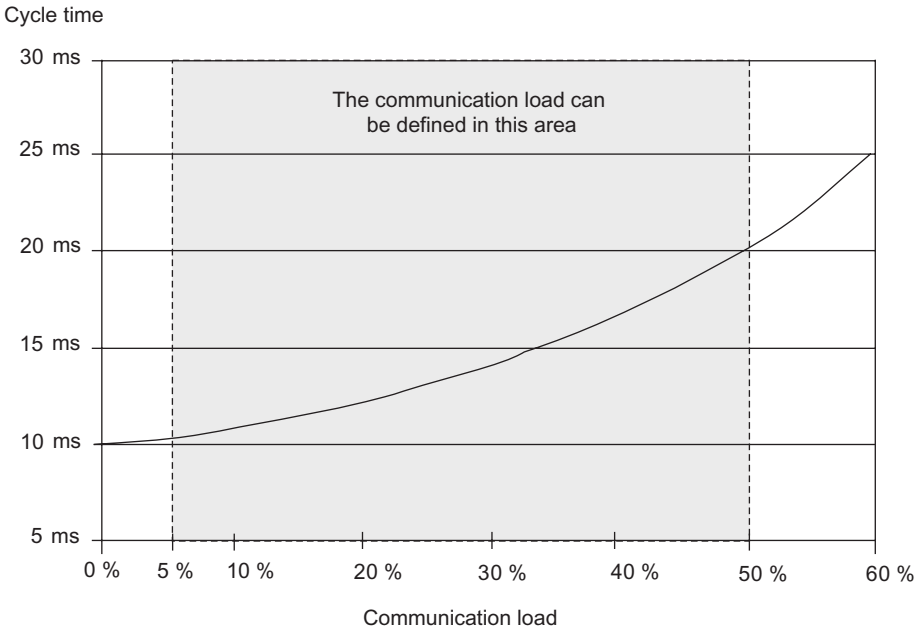
In your hardware configuration, you have specified a communication load of 20 %. The calculated cycle time is 10 ms. Using the above formula, the cycle time is extended by the factor 1.25.

Example: 50 % communication load

In your hardware configuration, you have specified a communication load of 50%. The calculated cycle time is 10 ms. Using the above formula, the cycle time is extended by the factor 2.

Physical cycle time depending on communication load

The figure below describes the non-linear dependency of the physical cycle time on communication load. In our sample we have chosen a cycle time of 10 ms.



Influence on the physical cycle time

From the statistical viewpoint, asynchronous events—such as interrupts—occur more frequently within the OB1 cycle when the cycle time is extended as a result of communication load. This further extends the OB1 cycle. This extension depends on the number of events that occur per OB1 cycle and the time required to process these events.

Note

Change the value of the "communication load" parameter to check the effects on the cycle time at system runtime. You must consider the communication load when you set the maximum cycle time, otherwise timing errors may occur.

Tips

- Use the default setting wherever possible.
- Increase this value only if the CPU is used primarily for communications and if the user program is not time critical.
- In all other situations you should only reduce this value.

5.2.5 Cycle time extension as a result of testing and commissioning functions

Runtimes

The runtimes of the testing and commissioning functions are operating system runtimes, so they are the same for every CPU. Initially, there is no difference between process mode and testing mode. How the cycle time is extended as a result of active testing and commissioning functions is shown in the table below.

Table 5-9 Cycle time extension as a result of testing and commissioning functions

Function	CPU 31xC/ CPU 31x
Status variable	50 µs for each variable
Control variable	50 µs for each variable
Block status	200 µs for each monitored line

Configuration during parameter assignment

For **process operation**, the maximum permissible cycle load by communication is not specified in "Cycle load by communication", but rather in "Maximum permitted increase of cycle time as a result of testing functions during process operation". Thus, the configured time is monitored absolutely in process mode and data acquisition is stopped if a timeout occurs. This is how STEP 7 stops data requests in loops before a loop ends, for example. When running in **Testing mode**, the complete loop is executed in every cycle. This can significantly increase cycle time.

5.2.6 Cycle extension through Component Based Automation (CBA)

By default, the operating system of your CPU updates the PROFINET interface as well as the DP interconnections at the cycle control point. However, if you deactivated these automatic updates during configuration (e.g. to obtain improved capabilities of influencing the time behavior of the CPU), you must perform the update manually. This is done by calling SFCs 112 to 114 at the appropriate times.

Reference

Information about SFC 112 to 114 is available in the *STEP 7 Online Help*.

Extending the OB1 cycle time

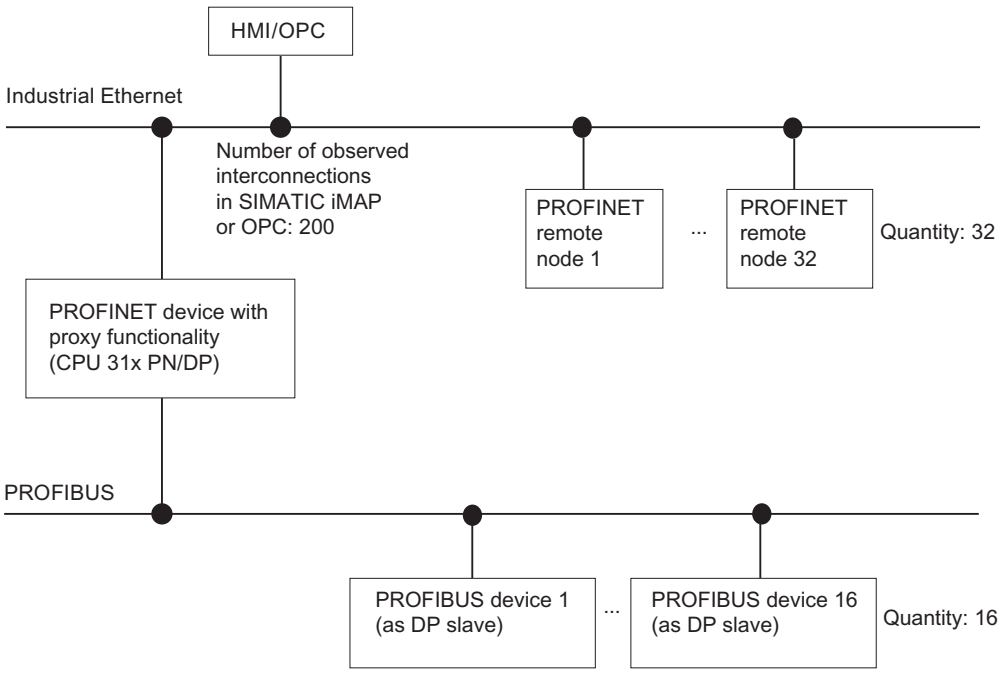
The OB1 cycle is extended by

- Increasing the number of PROFINET interconnections,
- Increasing the number of remote partners,
- Increasing the data volume and
- Incrasing the transfer frequency

Note

The use of CBA with cyclical PROFINET interconnections requires the use of switches to maintain the performance data. 100-Mbit full-duplex operation is mandatory with cyclical PROFINET interconnections.

The following graphic shows the configuration that was used for the measurements.



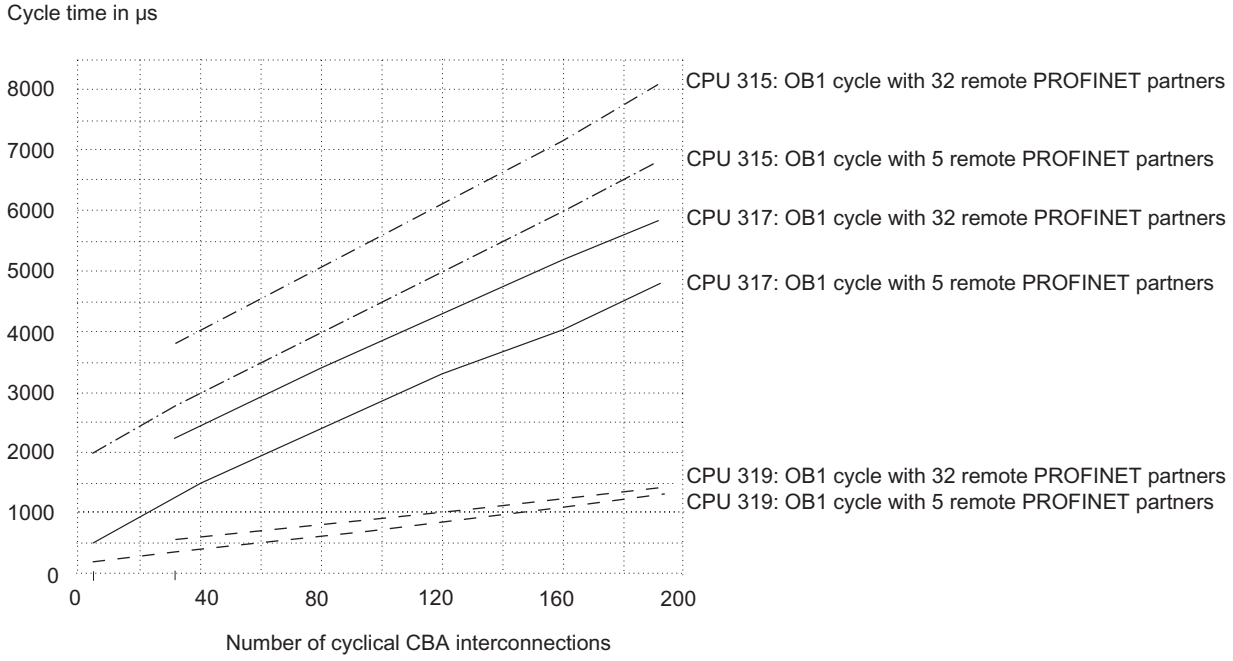
The upper graphic displays Incoming/outgoing remote connections	Quantity for CPU 315 and CPU 317	Quantity for CPU 319
Cyclical interconnection via Ethernet	200, scan cycle rate: Intervals of 10 ms	300, scan cycle rate: Intervals of 10 ms
Acyclic interconnection via Ethernet	100, scan cycle rate: Intervals of 500 ms	100, scan cycle rate: Intervals of 200 ms
Interconnections from the PROFINET device with proxy functionality to the PROFIBUS devices	16 x 4	16 x 4
Interconnections of PROFIBUS devices among each other	16 x 6	16 x 6

Additional marginal conditions

The maximum cycle load through communication in the measurement is 20 %.

The lower graphic shows that the OB1 cycle is influenced by increasing the cyclical PROFINET interconnections to remote partners at PROFINET:

Dependency of the OB1 cycle on the umber of interconnections



Base load through PROFIBUS devices

The 16 PROFIBUS devices with their interconnections among each other generate an **additional** base load of up to 1,0 ms.

Tips and notes

The upper graphic already includes the use of uniform values for the transfer frequency of all interconnections to a partner.

- The performance can drop by up to 50 % if the values are distributed to different frequency levels.
- The use of data structures and arrays in an interconnection instead of many single interconnections with simple data structures increases the performance.

5.3 Response time

5.3.1 Overview

Definition of response time

The response time is the time between the detection of an input signal and the change of a linked output signal.

Fluctuation width

The physical response time lies between the shortest and the longest response time. You must always reckon with the longest response time when configuring your system.

The shortest and longest response times are shown below, to give you an idea of the fluctuation width of the response time.

Factors

The response time depends on the cycle time and following factors:

- Delay of the inputs and outputs of signal modules or integrated I/O.
- Additional update times for PROFINET IO
- additional DP cycle times on PROFIBUS DP
- Execution in the user program

Reference

- The delay times are located in the specifications of the signal modules (*Module data* Reference Manual).

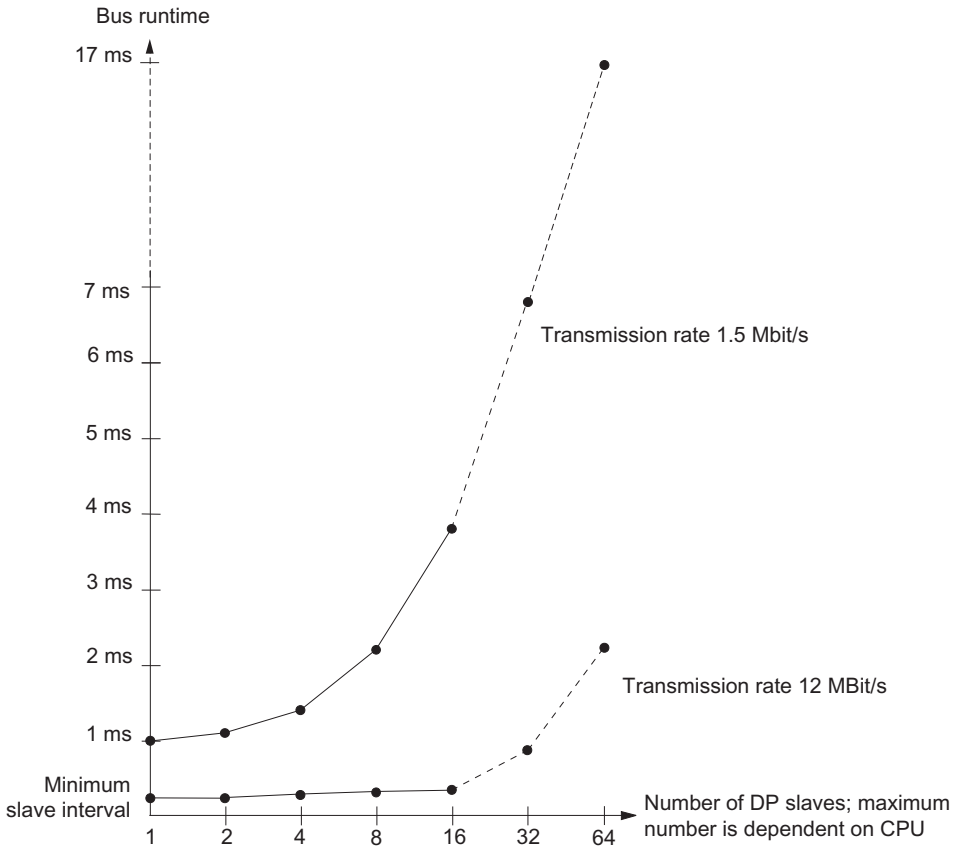
Update times for PROFINET IO

If you configured your PROFINET IO system in STEP 7, STEP 7 calculates the update time for PROFINET IO. You can then view the PROFINET IO update times on your PG.

DP cycle times in the PROFIBUS DP network

If you have configured your PROFIBUS DP master system in STEP 7, STEP 7 calculates the typical DP cycle time to be expected. You can then view the DP cycle time of your configuration on the PG.

The figure below gives you an overview of the DP cycle time. In this example, let us assume that the data of each DP slave has an average length of 4 bytes.

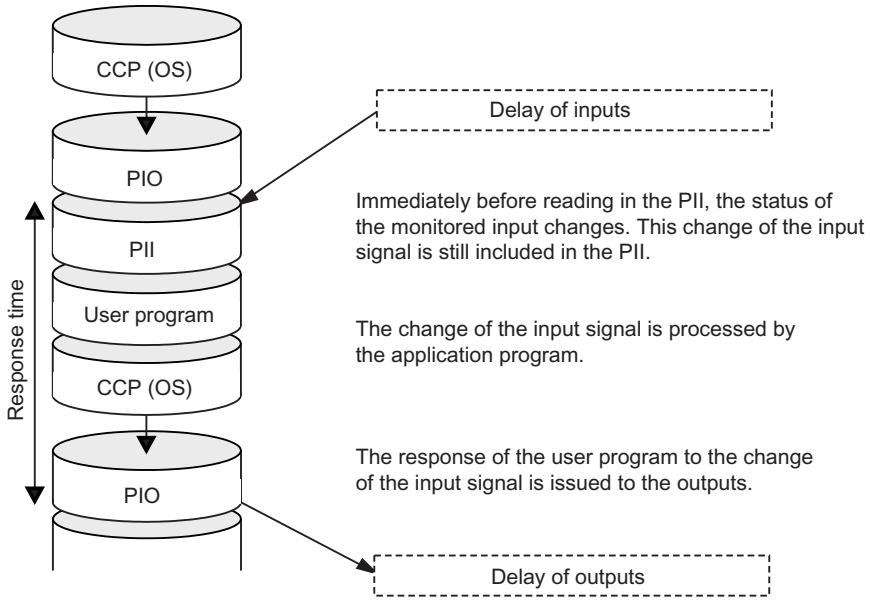


With multi-master operation on a PROFIBUS-DP network, you must make allowances for the DP cycle time at each master. That is, you will have to calculate the times for each master separately and then add up the results.

5.3.2 Shortest response time

Conditions for the shortest response time

The figure below shows the conditions under which the shortest response time is reached.



Calculation

The (shortest) response time is the sum of:

Table 5-10 Formula: Shortest response time

	1 x process image transfer time for the inputs
+	1 x process image transfer time for the outputs
+	1 x program processing time
+	1 × operating system processing time at the SCC
+	I/O delay
=	**Shortest response time**

The result is equivalent to the sum of the cycle time plus the I/O delay times.

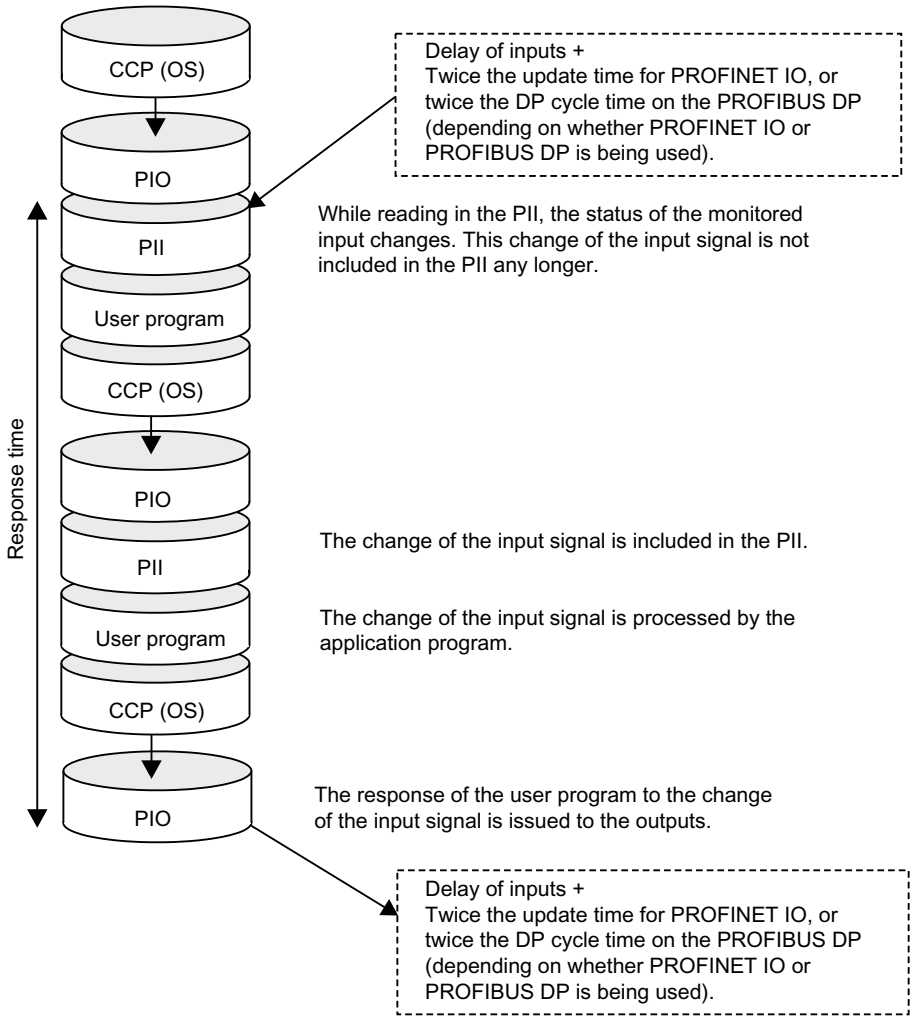
See also

Overview (Page 5-13)

5.3.3 Longest response time

Conditions for the longest response time

The figure below shows the conditions under which the longest response time is reached.



Calculation

The (longest) response time is the sum of:

Table 5-11 Formula: Longest response time

	2 x process image transfer time for the inputs
+	2 x process image transfer time for the outputs
+	2 x program processing time
+	2 × operating system processing time
+	2 x program processing time
+	4 x PROFINET IO update time (only if PROFINET IO is used.)
+	4 x DP cycle time on PROFIBUS DP (only if PROFIBUS DP is used.)
+	I/O delay
=	**Longest response time**

Equivalent to the sum of 2 x the cycle time + I/O delay time + 4 x times the PROFINET IO update time or 4 x times the DP cycle time on PROFIBUS DP

See also

Overview (Page 5-13)

5.3.4 Reducing the response time with direct I/O access

Reducing the response time

You can reach faster response times with direct access to the I/O in your user program, e.g. with

- L PIB or
- T PQW

you can partially avoid the response times described above.

Note

You can also achieve fast response times by using process interrupts.

See also

Shortest response time (Page 5-15)

Longest response time (Page 5-16)

5.4 Calculating method for calculating the cycle/response time

Introduction

This section gives you an overview of how to calculate the cycle/response time.

Cycle time

1. Determine the user program runtime with the help of the *Instruction list*.
2. Multiply the calculated value by the CPU-specific factor from the table *Extension of user program processing time*.
3. Calculate and add the process image transfer time. Corresponding guide values are found in table *Data for calculating process image transfer time*.
4. Add the processing time at the scan cycle checkpoint. Corresponding guide values are found in the table *Operating system processing time at the scan cycle checkpoint*.
5. Include the extensions as a result of testing and commissioning functions as well as cyclical PROFINET interconnections in your calculation. These values are found in the table *Cycle time extension due to testing and commissioning functions.* The final result is the cycle time.

Extension of the cycle time as a result of interrupts and communication load

100 / (100 – configured communication load in %)

1. Multiply the cycle time by the factor as in the formula above.
2. Calculate the runtime of interrupt processing program sections with the help of the instruction list. Add the corresponding value from the table below.
3. Multiply both values by the CPU-specific extension factor of the user program processing time.
4. Add the value of the interrupt-processing program sequences to the theoretical cycle time, multiplied by the number of triggering (or expected) interrupt events within the cycle time. The result is an approximation of the **physical cycle time**. Note down the result.

See also

Cycle extension through Component Based Automation (CBA) (Page 5-10)

Response time

Table 5-12 Calculating the response time

Shortest response time	Longest response time
-	Multiply the physical cycle time by factor 2.
Now add I/O delay.	Now add the I/O delay plus the DP cycle times on PROFIBUS-DP or the PROFINET IO update times.
The result is the shortest response time.	The result is the longest response time.

See also

Longest response time (Page 5-16)
Shortest response time (Page 5-15)
Calculating the cycle time (Page 5-4)
Cycle extension through Component Based Automation (CBA) (Page 5-10)

5.5 Interrupt response time

5.5.1 Overview

Definition of interrupt response time

The interrupt response time is the time that expires between the first occurrence of an interrupt signal and the call of the first interrupt OB instruction. Generally valid: Higher-priority interrupts take priority. This means that the interrupt response time is increased by the program processing time of the higher-priority interrupt OBs and the interrupt OBs of equal priority which have not yet been executed (queued).

Process/diagnostic interrupt response times of the CPUs

Table 5-13 Process and diagnostic interrupt response times

	Process interrupt response times			Diagnostic interrupt response times	
CPU	External min.	External Max.	Integrated I/O Max.	Min.	Max.
CPU 312	0.5 ms	0,8 ms	-	0.5 ms	1,0 ms
CPU 312C	0.5 ms	0,8 ms	0,6 ms	0.5 ms	1,0 ms
CPU 313C	0,4 ms	0,6 ms	0.5 ms	0,4 ms	1,0 ms
CPU 313C-2	0,4 ms	0,7 ms	0.5 ms	0,4 ms	1,0 ms
CPU 314	0,4 ms	0,7 ms	-	0,4 ms	1,0 ms
CPU 314C-2	0,4 ms	0,7 ms	0.5 ms	0,4 ms	1,0 ms
CPU 315-2 DP CPU 315-2 PN/DP	0,4 ms	0,7 ms	-	0,4 ms	1,0 ms
CPU 317-2 DP CPU 317-2 PN/DP	0,2 ms	0,3 ms	-	0,2 ms	0,3 ms
CPU 319-3 PN/DP	0.06 ms	0.10 ms	-	0.09 ms	0.12 ms

Calculation

The formula below show how you can calculate the minimum and maximum interrupt response times.

Table 5-14 Process and diagnostic interrupt response times

Calculation of the minimum and maximum interrupt reaction time	
Minimum interrupt reaction time of the CPU + Minimum interrupt reaction time of the signal modules + PROFINET IO update time (only if PROFINET IO is used.) + DP cycle time on PROFIBUS DP (only if PROFIBUS DP is used.) = Quickest interrupt reaction time	Maximum interrupt reaction time of the CPU + Maximum interrupt reaction time of the signal modules + 2 x PROFINET IO update time (only if PROFINET IO is used.) + 2 x DP cycle time on PROFIBUS DP (only if PROFIBUS DP is used.) The maximum interrupt reaction time is longer when the communication functions are active. The extra time is calculated using the following formula: **tv: 200 µs + 1000 µs x n%** n = Setting of the cycle load as a result of communication

Signal modules

The **process interrupt response time** of signal modules is determined by the following factors:

- Digital input modules

  Process interrupt response time = internal interrupt preparation time + input delay

  You will find these times in the data sheet for the respective digital input module.

- Analog input modules

  Process interrupt response time = internal interrupt preparation time + input delay

  The internal interrupt preparation time for analog input modules can be neglected. The conversion times can be found in the data sheet for the individual analog input modules.

The **diagnostic interrupt response time** of signal modules is equivalent to the period that expires between the time a signal module detects a diagnostic event and the time this signal module triggers the diagnostic interrupt. This short time can be neglected.

Process interrupt processing

Process interrupt processing begins after process interrupt OB40 is called. Higher-priority interrupts stop process interrupt processing. Direct I/O access is executed during runtime of the instruction. After process interrupt processing has terminated, cyclic program execution continues or further interrupt OBs of equal or lower priority are called and processed.

See also

Overview (Page 5-1)

5.5.2 Reproducibility of Time-Delay and Watchdog Interrupts

Definition of "Reproducibility"

Delay interrupt:

The period that expires between the call of the first instruction in the interrupt OB and the programmed time of interrupt.

Watchdog interrupt:

The fluctuation width of the interval between two successive calls, measured between the respective initial instructions of the interrupt OBs.

Reproducibility

The following times apply for the CPUs described in this manual, with the exception of CPU 319

- Delay interrupt: +/- 200 µs
- Watchdog interrupt: +/- 200 µs

The following times apply in the case of CPU 319:

- Delay interrupt: +/- 140 µs
- Watchdog interrupt: +/- 88 µs

These times only apply if the interrupt can actually be executed at this time and if not interrupted, for example, by higher-priority interrupts or queued interrupts of equal priority.

5.6 Sample calculations

5.6.1 Example of cycle time calculation

Design

You have configured an S7300 and equipped it with following modules in rack "0":

- a CPU 314C-2
- 2 digital input modules SM 321; DI 32 x 24 VDC (4 bytes each in the PI)
- 2 digital output modules SM 322; DO 32 x 24 VDC/0.5 A (4 bytes each in the PI)

User Program

According to the Instruction List, the user program runtime is 5 ms. There is no active communication.

Calculating the cycle time

The cycle time for the example results from the following times:

- User program execution time:

  approx. 5 ms x CPU-specific factor 1.10 = approx. 5.5 ms
- Process image transfer time

  Process image of inputs: 100 µs + 8 Byte x 37 µs = approx. 0.4 ms

  Process image of outputs: 100 µs + 8 Byte x 37 µs = approx. 0.4 ms
- Operating system runtime at scan cycle checkpoint:

  Approx. 0.5 ms

Cycle time = 5.5 ms + 0.4 ms + 0.4 ms + 0.5 ms = 6.8 ms.

Calculation of the actual cycle time

- There is no active communication.
- There is no interrupt handling.

Hence, the **physical cycle time** is 6 ms.

Calculating the longest response time

Longest response time:

6.8 ms x 2 = 13.6 ms.

- I/O delay can be neglected.
- Neither PROFIBUS DP, nor PROFINET IO are being used, so you do not have to make allowances for any DP cycle times on PROFIBUS DP or for PROFINET IO update times.
- There is no interrupt handling.

5.6.2 Sample of response time calculation

Design

You have configured an S7300 and equipped it with the following modules in two racks:

- a CPU 314C-2

  Configuring the cycle load as a result of communication: 40 %
- 4 digital input modules SM 321; DI 32 x 24 VDC (4 bytes each in the PI)
- 3 digital output modules SM 322; DO 16 x 24 VDC/0.5 A (2 bytes each in the PI)
- 2 analog input modules SM 331; AI 8 x 12-bit (not in the PI)
- 2 analog output modules SM 332; AO 4 x 12 bit (not in the PI)

User Program

According to the instruction list, the user program runtime is 10.0 ms.

Calculating the cycle time

The cycle time for the example results from the following times:

- User program execution time:

  approx. 10 ms x CPU-specific factor 1.10 = approx. 11 ms
- Process image transfer time

  Process image of inputs: 100 µs + 16 bytes x 37 µs = approx. 0.7 ms

  Process image of outputs: 100 µs + 6 bytes x 37 µs = approx. 0.3 ms
- Operating system runtime at scan cycle checkpoint:

  Approx. 0.5 ms

The sum of the listed times is equivalent to the cycle time:

Cycle time = 11.0 ms + 0.7 ms + 0.3 ms + 0.5 ms = 12.5 ms.

Calculation of the actual cycle time

Under consideration of communication load:

12.5 ms x 100 / (100-40) = 20.8 ms.

Thus, under consideration of time-sharing factors, the **actual cycle time** is **21 ms**.

Calculation of the longest response time

- Longest response time = 21 ms x 2 = 42 ms.
- I/O delay
  - The maximum delay of the input digital module SM 321; DI 32 x 24 VDC is **4.8 ms** per channel.
  - The output delay of the digital output module SM 322; DO 16 x 24 VDC/0.5 A **can be neglected**.
  - The analog input module SM 331; AI 8 x 12 bit was configured for an interference suppression at 50 Hz. The result is a conversion time of 22 ms per channel. With the eight active channels, the result is a cycle time of **176 ms** for the analog input module.
  - The analog output module SM 332; AO 4 x 12-bit was programmed for the measuring range of 0 ...10 Hz. This gives a conversion time of 0.8 ms per channel. Since 4 channels are active, the result is a cycle time of 3.2 ms. A settling time of 0.1 ms for a resistive load must be added to this value. The result is a response time of **3.3 ms** for an analog output.
- Neither PROFIBUS DP, nor PROFINET IO are being used, so you do not have to make allowances for any DP cycle times on PROFIBUS DP or for PROFINET IO update times.

- Response times plus I/O delay:
  - **Case 1:** An output channel of the digital output module is set when a signal is received at the digital input. The result is a response time of:

    Response time = 42 ms + 4.8 ms = 46.8 ms.
  - **Case 2:** An analog value is fetched, and an analog value is output. The result is a response time of:

    Longest response time = 42 ms + 176 ms + 3.3 ms = 221.3 ms.

5.6.3 Example of interrupt response time calculation

Design

You have assembled an S7-300, consisting of one CPU 314C-2 and four digital modules in the CPU rack. One of the digital input modules is an SM 321; DI 16 x 24 VDC; with process/diagnostic interrupt function.

You have enabled only the process interrupt in your CPU and SM parameter configuration. You decided not to use time-controlled processing, diagnostics or error handling. You have configured a 20% communication load on the cycle.

You have configured a delay of 0.5 ms for the inputs of the DI module.

No activities are required at the scan cycle checkpoint.

Calculation

In this example, the process interrupt response time is based on following time factors:

- Process interrupt response time of CPU 314C-2: approx. 0,7 ms
- Extension by communication according to the formula:

  200 µs + 1000 µs x 20 % = 400 µs = 0.4 ms
- Process interrupt response time of SM 321; DI 16 x 24 VDC:
  - Internal interrupt preparation time: 0.25 ms
  - Input delay: 0.5 ms
- Neither PROFIBUS DP, nor PROFINET IO are being used, so you do not have to make allowances for any DP cycle times on PROFIBUS DP or for PROFINET IO update times.

The process interrupt response time is equivalent to the sum of the listed time factors:

Process interrupt response time = 0.7 ms + 0.4 ms + 0.25 ms + 0.5 ms = **approx. 1.85 ms**.

This calculated process interrupt response time expires between the time a signal is received at the digital input and the call of the first instruction in OB40.

Technical data of CPU 31xC

6

6.1 General technical data

6.1.1 Dimensions of CPU 31xC

Each CPU features the same height and depth, only the width dimensions differ.

- Height: 125 mm
- Depth: 115 mm, or 180 mm with opened front cover.

Width of CPU

CPU	Width
CPU 312C	80 mm
CPU 313C	120 mm
CPU 313C-2 PtP	120 mm
CPU 313C-2 DP	120 mm
CPU 314C-2 PtP	120 mm
CPU 314C-2 DP	120 mm

6.1.2 Technical specifications of the Micro Memory Card (MMC)

Plug-in SIMATIC Micro Memory Card (MMC)

The following memory modules are available:

Table 6-1 Available SIMATIC Micro Memory Cards

Type	Order number	Required for a firmware update via SIMATIC Micro Memory Card
MMC 64k	6ES7 953-8LFxx-0AA0	–
MMC 128k	6ES7 953-8LGxx-0AA0	–
MMC 512k	6ES7 953-8LJxx-0AA0	–
MMC 2M	6ES7 953-8LLxx-0AA0	Minimum requirement for CPUs without DP interface
MMC 4M	6ES7 953-8LMxx-0AA0	Minimum requirement for CPUs without DP interface (except CPU 319)
MMC 8M [1]	6ES7 953-8LPxx-0AA0	Minimum requirements for the CPU 319

[1] If you plug in the CPU 312C or CPU 312, you cannot use this SIMATIC Micro Memory Card.

Maximum number of loadable blocks on the SIMATIC Micro Memory Card

Number of blocks that can be stored on the SIMATIC Micro Memory Card depends on the capacity of the SIMATIC Micro Memory Card being used The maximum number of blocks that can be loaded is therefore limited by the capacity of your MMC (including blocks generated with the "CREATE DB" SFC)

Table 6-2 Maximum number of loadable blocks on the SIMATIC Micro Memory Card

Size of SIMATIC Micro Memory Card	Maximum number of blocks that can be loaded
64 KB	768
128 KB	1024
512 KB	Here the maximum number of blocks that can be loaded for the specific CPU is less than the number of blocks that can be stored on the SIMATIC Micro Memory Card. Refer to the corresponding specifications of a specific CPU to determine the maximum number of blocks that can be loaded.
2 MB	
4 MB	
8 MB	

6.2 CPU 312C

Technical data

Table 6-3 Technical data of CPU 312C

Technical data	
CPU and version	
Order number	6ES7 312-5BD01-0AB0
• Hardware version	01
• Firmware version	V2.0
• Associated programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	
RAM	
• Integrated	16 KB
• Expandable	No
Load memory	Plugged in with MMC (Max. 4 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	Guaranteed by MMC (maintenance-free)
Execution times	
Processing times of	
• Bit operations	Min. 0.2 µs
• Word instructions	Min. 0.4 µs
• Fixed-point arithmetic	Min. 5 µs
• Floating-point arithmetic	Min. 6 µs
Timers/counters and their retentivity	
S7 counters	128
• Retentive address areas	Configurable
• Default	from C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
S7 timers	128
• Retentive address areas	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)

Technical data	
Data areas and their retentivity	
Flag bits	128 bytes
• Retentive address areas	Configurable
• Default retentivity	MB0 to MB15
Clock flag bits	8 (1 byte per flag bit)
Data blocks	Max. 511 (in the 1 to 511 range of numbers)
• Size	Max. 16 KB
Local data per priority class	Max. 256 bytes
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	see the Instruction List
• Size	Max. 16 KB
Nesting depth	
• Per priority class	8
• additional within an error OB	4
FBs	
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	Max. 16 KB
FCs	
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	Max. 16 KB
Address areas (I/O)	
Total I/O address area	Max. 1024 bytes/1024 bytes (can be freely addressed)
I/O process image	128 bytes/128 bytes
Digital channels	Max. 256
• Of those central	Max. 256
• Integrated channels	10 DI / 6 DO
Analog channels	Max. 64
• Of those central	Max. 64
• Integrated channels	None
Assembly	
Racks	Max. 1
Modules per rack	Max. 8
Number of DP masters	
• Integrated	None
• Via CP	4

Technical data	
Number of function modules and communication processors you can operate	
• FM	Max. 8
• CP (PtP)	Max. 8
• CP (LAN)	Max. 4
Time-of-day	
Real-time clock	Yes (SW clock)
• Buffered	No
• Accuracy	Deviation per day < 10 s
• Behavior of the realtime clock after POWER OFF	The clock keeps running, continuing at the time-of-day it had when power was switched off.
Operating hours counter	1
• Number	0
• Value range	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	Yes; must be manually restarted after every restart
Clock synchronization	Yes
• In the PLC	Master
• On MPI	Master/slave
S7 signaling functions	
Number of stations that can be logged on for signaling functions	Max. 6 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	Max. 20
Testing and commissioning functions	
Status/control variables	Yes
• Variables	Inputs, outputs, memory bits, DBs, timers, counters
• Number of variables – Of those as status variable – Of those as control variable	Max. 30 Max. 30 Max. 14
Forcing	Yes
• Variables	Inputs, outputs
• Number of variables	Max. 10
Block status	Yes
Single step	Yes
Breakpoints	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	Max. 100

Technical data	
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	4
• Number of GD packets – Sending stations – Receiving stations	Max. 4 Max. 4 Max. 4
• Length of GD packets – Consistent data	Max. 22 bytes 22 bytes
S7 basic communication	Yes
• User data per job • Consistent data	Max. 76 bytes 76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	
• As server	Yes
• User data per job – Consistent data	Max. 180 bytes (with PUT/GET) 64 bytes
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	Max. 6
can be used for	
• PG communication – Reserved (default) – Configurable	Max. 5 1 From 1 to 5
• OP communication – Reserved (default) – Configurable	Max. 5 1 From 1 to 5
• S7-based communication – Reserved (default) – Configurable	Max. 2 2 from 0 to 2
Routing	No
Interfaces	
1st interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	No
Interface power supply (15 to 30 VDC)	Max. 200 mA
Functionality	
• MPI	Yes
• PROFIBUS DP	No
• Point-to-point communication	No

Technical data	
MPI	
Services	
• PG/OP communication	Yes
• Routing	No
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication – As server – As client	 Yes No
• Transmission rates	Max. 187.5 kbps
Programming	
Programming language	LAD/FBD/STL
Available instructions	see the Instruction List
Nesting levels	8
System functions (SFCs)	see the Instruction List
System function blocks (SFBs)	see the Instruction List
User program security	Yes
Integrated I/O	
• Default addresses of the integrated – Digital inputs – Digital outputs	 124.0 to 125.1 124.0 to 124.5
Integrated functions	
Counters	2 channels (see the Manual *Technological Functions*)
Frequency counters	2 channels, Max. 10 kHz (see the Manual *Technological Functions*)
Pulse outputs	2 channels for pulse width modulation, Max. 2.5 kHz (see the Manual *Technological Functions*)
Controlled positioning	No
Integrated "Controlling" SFB	No
Dimensions	
Mounting dimensions W x H x D (mm)	80 x 125 x 130
Weight	409 g
Voltages and currents	
Power supply (rated value)	24 VDC
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	Typically 60 mA
Inrush current	Typically 11 A
Power consumption (nominal value)	500 mA
I^2t	0.7 A^2s
External fusing of power supply lines (recommended)	LS switch Type C min. 2 A, LS switch Type B min. 4 A
Power loss	Typically 6 W

Reference

In Chapter *Specifications of the integrated I/O* you can find

- the specifications of integrated I/Os under *Digital inputs of CPUs 31xC* and *Digital outputs of CPUs 31xC*.
- the block diagrams of the integrated I/Os under *Arrangement and usage of integrated I/Os*.

6.3 CPU 313C

Technical data

Table 6-4 Technical data of CPU 313C

Technical data	
CPU and version	
Order no. [MLFB]	6ES7 313-5BE01-0AB0
• Hardware version	01
• Firmware version	V2.0.0
• Associated programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	
Work memory	
• Integrated	32KB
• Expandable	No
Load memory	Plugged in with MMC (Max. 8 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	Guaranteed by MMC (maintenance-free)
Execution times	
Processing times of	
• Bit operations	Min. 0.1 µs
• Word instructions	Min. 0.2 µs
• Fixed-point arithmatic	Min. 2 µs
• Floating-point arithmatic	Min. 3 µs
Timers/counters and their retentive address areas	
S7 counters	256
• Retentive address areas	Configurable
• Default	From C 0 to C 7
• Counting range	0 to 999

Technical data	
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
S7 timers	256
• Retentive address areas	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
Data areas and their retentive address areas	
Bit memory	256 bytes
• Retentive address areas	Configurable
• Default retentive address areas	MB0 to MB15
Clock memory	8 (1 memory byte)
Data blocks	Max. 511 (in the 1 to 511 range of numbers)
• Size	Max. 16 KB
Local data per priority class	Max. 510 bytes
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	see the Instruction List
• Size	Max. 16 KB
Nesting depth	
• Per priority class	8
• Additional within an error OB	4
FBs	
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	Max. 16 KB
FCs	
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	Max. 16 KB
Address areas (I/O)	
Total I/O address area	Max. 1024 bytes/1024 bytes (can be freely addressed)
I/O process image	128 bytes / 128 bytes

Technical data	
Digital channels	Max. 1016
• Centralized	Max. 992
• Integrated channels	24 DI / 16 DO
Analog channels	Max. 253
• Centralized	Max. 248
• Integrated channels	4 + 1 AI / 2 AO
Removal	
Module rack	Max. 4
Modules per rack	Max. 8; Max. 7 in rack 3
Number of DP masters	
• Integrated	None
• Via CP	4
Operable function modules and communication processors	
• FM	Max. 8
• CP (PtP)	Max. 8
• CP (LAN)	Max. 6
Time	
Clock	Yes (hardware clock)
• Buffered	Yes
• Buffered period	Typically 6 weeks (at an ambient temperature of 40 °C)
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.
• Accuracy	Deviation per day < 10 s
Operating hours counter	1
• Number	0
• Value range	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	Yes; must be manually restarted after every restart
Time synchronization	Yes
• In the PLC	Master
• On MPI	Master/slave
S7 message functions	
Number of stations that can be logged on for signaling functions	Max. 8 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	Max. 20

Technical data	
Test and startup functions	
Status/control variables	Yes
• Variables	Inputs, outputs, memories, DBs, timers, counters
• Number of variables – of those as status variable – of those as control variable	Max. 30 Max. 30 Max. 14
Force	Yes
• Variables	Inputs, outputs
• Number of variables	Max. 10
Block status	Yes
Single-step	Yes
Breakpoints	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	Max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	4
• Number of GD packets – Sender – Receiver	Max. 4 Max. 4 Max. 4
• Size of GD packets – Consistent data	Max. 22 bytes 22 bytes
S7 basic communication	Yes
• User data per job – Consistent data	Max. 76 bytes 76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	
• As server	Yes
• As client	Yes (via CP and loadable FBs)
• User data per job – Consistent data	Max. 180 bytes (with PUT/GET) 64 bytes
S5compatible communication	Yes (via CP and loadable FCs)
Number of connections	Max. 8
Can be used for	
• PG communication – Reserved (default) – Configurable	Max. 7 1 From 1 to 7
• OP communication – Reserved (default) – Configurable	Max. 7 1 From 1 to 7

Technical data	
• S7 basic communication – Reserved (default) – Configurable	Max. 4 4 From 0 to 4
Routing	No
interfaces	
1st interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	No
Interface power supply (15 to 30 VDC)	Max. 200 mA
Functionality	
• MPI	Yes
• PROFIBUS DP	No
• PtP communication	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	No
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication – As server – As client	 Yes No (but with CP and loadable FB)
• Transmission rates	Max. 187.5 kbps
Programming	
Programming language	LAD/FBD/STL
Instruction set	see the Instruction List
Nesting levels	8
System functions (SFC)	see the Instruction List
System function blocks (SFB)	see the Instruction List
User program protection	Yes
Integrated I/O	
• Default addresses of the integrated – Digital inputs – Digital outputs – Analog inputs – Analog outputs	 124.0 to 126.7 124.0 to 125.7 752 to 761 752 to 755
Integrated functions	
Counters	3 channels (see manual *Technological Functions*)
Frequency counter	3 channels up to Max. 30 kHz (see the *Technological Functions* manual)
Pulse outputs	3 channels pulse-width modulation up to Max. 2,5 kHz (see *Technological Functions* manual)

Technical data	
Controlled positioning	No
Integrated "Controlling" SFB	PID controller (see the *Technological Functions* manual)
Dimensions	
Mounting dimensions W x H x D (mm)	120 x 125 x 130
Weight	660 g
Voltages, currents	
Power supply (rated value)	DC 24 V
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	Typically 150 mA
Making current	typ. 11 A
Power consumption (nominal value)	700 mA
I^2t	0,7 A^2s
External fusing of power supply lines (recommended)	LS switch Type C min. 2 A, LS switch Type B min. 4 A,
Power loss	Typically 14 W

Reference

In Chapter *Specifications of the integrated I/O* you can find

- the specifications of integrated I/O under *Digital inputs of CPUs 31xC*, *Digital outputs of CPUs 31xC, Analog inputs of CPUs 31xC* and *Analog outputs of CPUs 31xC*.
- the block diagrams of the integrated I/Os under *Arrangement and usage of integrated I/Os*.

6.4 CPU 313C-2 PtP and CPU 313C-2 DP

Technical Data

Table 6-5 Technical data for CPU 313C-2 PtP/ CPU 313C-2 DP

Technical data		
	CPU 313C-2 PtP	**CPU 313C-2 DP**
CPU and version	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Order no. [MLFB]	6ES7 313-6BE01-0AB0	6ES7 313-6CE01-0AB0
• Hardware version	01	01
• Firmware version	V2.0.0	V2.0.0
Associated programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Work memory		
• Integrated	32KB	
• Expandable	No	
Load memory	Plugged in with MMC (Max. 8 MB)	
Data storage life on the MMC (following final programming)	At least 10 years	
Buffering	Guaranteed by MMC (maintenance-free)	
Execution times	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Processing times of		
• Bit operations	Min. 0.1 µs	
• Word instructions	Min. 0.2 µs	
• Fixed-point arithmatic	Min. 2 µs	
• Floating-point arithmatic	Min. 3 µs	
Timers/counters and their retentive address areas	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
S7 counters	256	
• Retentive address areas	Configurable	
• Preset	From C 0 to C 7	
• Counting range	0 to 999	
IEC Counters	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
S7 timers	256	
• Retentive address areas	Configurable	
• Preset	Not retentive	
• Timer range	10 ms to 9990 s	

Technical data		
	CPU 313C-2 PtP	**CPU 313C-2 DP**
IEC timers	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
Data areas and their retentive address areas	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Bit memory	256 bytes	
• Retentive address areas	Configurable	
• Preset retentive address areas	MB0 to MB15	
Clock memory	8 (1 memory byte)	
Data blocks	Max. 511 (in the 1 to 511 range of numbers)	
• Size	Max. 16 KB	
Local data per priority class	Max. 510 bytes	
Blocks	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.	
OBs	see the Instruction List	
• Size	Max. 16 KB	
Nesting depth		
• Per priority class	8	
• Additional within an error OB	4	
FBs		
• Number, Max.	1024 (in the 0 to 2047 range of numbers)	
• Size	Max. 16 KB	
FCs		
• Number, Max.	1024 (in the 0 to 2047 range of numbers)	
• Size	Max. 16 KB	
Address areas (I/O)	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Total I/O address area	Max. 1024 bytes/1024 bytes (can be freely addressed)	Max. 1024 bytes/1024 bytes (can be freely addressed)
• Distributed	None	Max. 1008 bytes
I/O process image	128 bytes / 128 bytes	128 bytes / 128 bytes
Digital channels	Max. 1008	Max. 8192
• Centralized	Max. 992	Max. 992
• Integrated channels	16 DI / 16 DO	16 DI / 16 DO
Analog channels	Max. 248	Max. 512
• Centralized	Max. 248	Max. 248
• Integrated channels	None	None

Technical data		
	CPU 313C-2 PtP	**CPU 313C-2 DP**
Removal	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Module rack	Max. 4	
Modules per rack	Max. 8; Max. 7 in rack 3	
Number of DP masters		
• Integrated	No	1
• Via CP	4	4
Operable function modules and communication processors		
• FM	Max. 8	
• CP (PtP)	Max. 8	
• CP (LAN)	Max. 6	
Time	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Clock	Yes (hardware clock)	
• Buffered	Yes	
• Buffered period	Typically 6 weeks (at an ambient temperature of 40 °C)	
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.	
• Accuracy	Deviation per day < 10 s	
Operating hours counter	1	
• Number	0	
• Value range	2^{31} hours (if SFC 101 is used)	
• Granularity	1 hour	
• Retentive	Yes; must be manually restarted after every restart	
Time synchronization	Yes	
• In the PLC	Master	
• On MPI	Master/slave	
S7 message functions	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Number of stations that can log in for signaling functions (e.g. OS)	Max. 8 (depends on the number of connections configured for PG / OP and S7 basic communication)	
Process diagnostics messages	Yes	
• Simultaneously enabled interrupt S blocks	Max. 20	
Test and startup functions	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Status/control variables	Yes	
• Variables	Inputs, outputs, bit memories, DBs, timers, counters	
• Number of variables – Of those as status variable – Of those as control variable	Max. 30 Max. 30 Max. 14	
Force	Yes	
• Variables	Inputs, outputs	
• Number of variables	Max. 10	

Technical data		
	CPU 313C-2 PtP	**CPU 313C-2 DP**
Block status	Yes	
Single-step	Yes	
Breakpoints	2	
Diagnostic buffer	Yes	
• Number of entries (not configurable)	Max. 100	
Communication functions	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
PG/OP communication	Yes	
Global data communication	Yes	
• Number of GD circuits	4	
• Number of GD packets – Sender – Receiver	Max. 4 Max. 4 Max. 4	
• Size of GD packets – Consistent data	Max. 22 bytes 22 bytes	
S7 basic communication	Yes (server)	
• User data per job – Consistent data	Max. 76 bytes 76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)	
S7 communication		
• As server	Yes	
• As client	Yes (via CP and loadable FBs)	
• User data per job – Consistent data	Max. 180 bytes (with PUT/GET) 64 bytes	
S5compatible communication	Yes (via CP and loadable FCs)	
Number of connections	Max. 8	
Can be used for		
• PG communication – Reserved (default) – Configurable	Max. 7 1 From 1 to 7	
• OP communication – Reserved (default) – Configurable	Max. 7 1 From 1 to 7	
• S7-based communication – Reserved (default) – Configurable	Max. 4 4 From 0 to 4	
Routing	No	Max. 4
interfaces	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
1st interface		
Type of interface	Integrated RS485 interface	
Physics	RS 485	
electrically isolated	No	
Interface power supply (15 to 30 VDC)	Max. 200 mA	

Technical data		
	CPU 313C-2 PtP	**CPU 313C-2 DP**
Functionality		
• MPI	Yes	
• PROFIBUS DP	No	
• Point-to-point connection	No	
MPI		
Services		
• PG/OP communication	Yes	
• Routing	No	Yes
• Global data communication	Yes	
• S7 basic communication	Yes	
• S7 communication – As server – As client	• • Yes • No (but via CP and loadable FBs)	
• Transmission rates	Max. 187.5 kbps	
2nd interface		
Type of interface	Integrated RS422/RS485 interface	Integrated RS485 interface
Physics	RS 422/485	RS 485
electrically isolated	Yes	Yes
Interface power supply (15 to 30 VDC)	No	Max. 200 mA
Number of connections	None	8
Functionality		
• MPI	No	No
• PROFIBUS DP	No	Yes
• Point-to-point connection	Yes	No
DP master		
Number of connections	–	8
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes
• Global data communication	–	No
• S7 basic communication	–	No
• S7 communication	–	No
• Constant bus cycle time	–	Yes
• SYNC/FREEZE	–	Yes
• Enable/disable DP slaves	–	Yes
• DPV1	–	Yes
• Transmission rates	–	Up to 12 Mbaud
• Number of DP slaves per station	–	Max. 32
• Address area	–	Max. 1 KB I / 1 KB O
• User data per DP slave	–	Max. 244 bytes I / 244 bytes O

Technical data		
	CPU 313C-2 PtP	**CPU 313C-2 DP**
DP slave		
Number of connections	–	8
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes (only if interface is active)
• Global data communication	–	No
• S7 basic communication	–	No
• S7 communication	–	No
• Direct data exchange	–	Yes
• Transmission rates	–	Up to 12 Mbaud
• Automatic baud rate search	–	Yes (only if interface is passive)
• Intermediate memory	–	244 bytes I / 244 bytes O
• Address areas	–	Max. 32, with Max. 32 bytes each
• DPV1	–	No
GSD file	–	The latest GSD file is available at: http://www.automation.siemens.com/csi/gsd
Point-to-point connection		
• Transmission rates	38.4 Kbaud half duplex 19.2 Kbaud full duplex	–
• Cable length	Max. 1200 m	–
• User program can control the interface	Yes	–
• The interface can trigger a break or an interrupt in the user program	Yes (message with break ID)	–
• Protocol driver	3964(R); ASCII	–
Programming	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Programming language	LAD/FBD/STL	
Instruction set	see the Instruction List	
Nesting levels	8	
System functions (SFC)	see the Instruction List	
System function blocks (SFB)	see the Instruction List	
User program protection	Yes	
Integrated I/O	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
• Default addresses of the integrated – Digital inputs – Digital outputs	 124.0 to 125.7 124.0 to 125.7	
Integrated functions		
Counters	3 channels (see the *Technological Functions* manual)	
Frequency counter	3 channels up to Max. 30 kHz (see the *Technological Functions* manual)	
Pulse outputs	3 channels pulse-width modulation up to Max. 2,5 kHz (see *Technological Functions* manual)	
Controlled positioning	No	

Technical data		
	CPU 313C-2 PtP	**CPU 313C-2 DP**
Integrated "Controlling" SFB	PID controller (see the *Technological Functions* manual)	
Dimensions	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Mounting dimensions W x H x D (mm)	120 x 125 x 130	
Weight	approx. 566 g	
Voltages, currents	**CPU 313C-2 PtP**	**CPU 313C-2 DP**
Power supply (rated value)	DC 24 V	
• Permitted range	20.4 V to 28.8 V	
Current consumption (no-load operation)	Typically 100 mA	
Making current	typ. 11 A	
Power consumption (nominal value)	700 mA	900 mA
I^2t	0,7 A^2s	
External fusing of power supply lines (recommended)	LS switch type B: min. 4 A, type C: min. 2 A	
Power loss	Typically 10 W	

Reference

In Chapter *Specifications of the integrated I/O* are found

- under *Digital inputs of CPUs 31xC* and *Digital outputs of CPUs 31xC* the technical data of integrated I/Os.
- the block diagrams of the integrated I/Os under *Arrangement and usage of integrated I/Os*.

6.5 CPU 314C-2 PtP and CPU 314C-2 DP

Technical Data

Table 6-6 Technical data of CPU 314C-2 PtP and CPU 314C-2 DP

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
CPU and version	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Order number	6ES7 314-6BF02-0AB0	6ES7 314-6CF02-0AB0
• Hardware version	01	01
• Firmware version	V2.0.0	V2.0.0
Associated programming package	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)	STEP 7 as of V 5.2 + SP 1 (please use previous CPU for STEP 7 V 5.1 + SP 3 or later)
Memory	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
RAM		
• Integrated	64 Kbytes	
• Expandable	No	
Load memory	Pluggable by means of SIMATIC Micro Memory Card (Max. 8 Mbytes)	
Data storage life on the MMC (following final programming)	At least 10 years	
Buffering	Guaranteed by MMC (maintenance-free)	
Execution times	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Processing times of		
• Bit operations	Min. 0.1 µs	
• Word instructions	Min. 0.2 µs	
• Fixed-point arithmetic	Min. 2 µs	
• Floating-point arithmetic	Min. 3 µs	
Timers/counters and their retentivity	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
S7 counters	256	
• Retentive address areas	Configurable	
• Default	from C0 to C7	
• Counting range	0 to 999	
IEC Counters	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
S7 timers	256	
• Retentive address areas	Configurable	
• Default	Not retentive	
• Timer range	10 ms to 9990 s	

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
IEC Timers	Yes	
• Type	SFB	
• Number	unlimited (limited only by RAM size)	
Data areas and their retentivity	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Flag bits	256 bytes	
• Retentive address areas	Configurable	
• Default retentivity	MB0 to MB15	
Clock flag bits	8 (1 byte per flag bit)	
Data blocks	Max. 511 (in the 1 to 511 range of numbers)	
• Size	Max. 16 Kbytes	
Local data per priority class	Max. 510 bytes	
Blocks	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.	
OBs	See the Instruction List	
• Size	Max. 16 KB	
Nesting depth		
• Per priority class	8	
• additional within an error OB	4	
FBs		
• Number, Max.	1024 (in the 0 to 2047 range of numbers)	
• Size	Max. 16 KB	
FCs		
• Number, Max.	1024 (in the 0 to 2047 range of numbers)	
• Size	Max. 16 KB	
Address areas (I/O)	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Total I/O address area	Max. 1024 bytes / 1024 bytes (can be freely addressed)	Max. 1024 bytes / 1024 bytes (can be freely addressed)
• Distributed	None	Max. 1000 bytes
I/O process image	128 bytes / 128 bytes	128 bytes / 128 bytes
Digital channels	Max. 1016	Max. 8192
• Centralized	Max. 992	Max. 992
• Integrated channels	24 DI / 16 DO	24 DI / 16 DO
Analog channels	Max. 253	Max. 512
• Centralized	Max. 248	Max. 248
• Integrated channels	4 + 1 AI / 2 AO	4 + 1 AI / 2 AO

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
Assembly	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Racks	Max. 4	
Modules per rack	Max. 8; Max. 7 in rack 3	
Number of DP masters		
• Integrated	No	1
• via CP	4	4
Number of function modules and communication processors you can operate		
• FM	Max. 8	
• CP (PtP)	Max. 8	
• CP (LAN)	Max. 10	
Time-of-day	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Real-time clock	Yes (HW clock)	
• Buffered	Yes	
• Buffered period	Typically 6 weeks (at an ambient temperature of 40 °C)	
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.	
• Accuracy	Deviation per day < 10 s	
Operating hours counter	1	
• Number	0	
• Value range	2^{31} hours (if SFC 101 is used)	
• Granularity	1 hour	
• Retentive	Yes; must be manually restarted after every restart	
Clock synchronization	Yes	
• In the PLC	Master	
• On MPI	Master/slave	
S7 signaling functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Number of stations that can log in for signaling functions (e.g. OS)	Max. 12 (depends on the number of connections configured for PG / OP and S7 basic communication)	
Process diagnostics messages	Yes	
• Simultaneously enabled interrupt S blocks	Max. 40	
Testing and commissioning functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Status/control variables	Yes	
• Variables	Inputs, outputs, memory bits, DBs, timers, counters	
• Number of variables – of those as status variable – of those as control variable	Max. 30 Max. 30 Max. 14	

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
Forcing	Yes	
• Variables	Inputs, outputs	
• Number of variables	Max. 10	
Block status	Yes	
Single step	Yes	
Breakpoints	2	
Diagnostic buffer	Yes	
• Number of entries (not configurable)	Max. 100	
Communication functions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
PG/OP communication	Yes	
Global data communication	Yes	
• Number of GD circuits	4	
• Number of GD packets – Sending stations – Receiving stations	Max. 4 Max. 4 Max. 4	
• Length of GD packets – Consistent data	Max. 22 bytes 22 bytes	
S7 basic communication	Yes	
• User data per job – Consistent data	Max. 76 bytes 76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)	
S7 communication		
• As server	Yes	
• as client	Yes (via CP and loadable FBs)	
• User data per job – Consistent data	Max. 180 bytes (with PUT/GET) 64 bytes	
S5-compatible communication	Yes (via CP and loadable FCs)	
Number of connections	Max. 12	
can be used for		
• PG communication – Reserved (default) – Configurable	Max. 11 1 From 1 to 11	
• OP communication – Reserved (default) – Configurable	Max. 11 1 From 1 to 11	
• S7-based communication – Reserved (default) – Configurable	Max. 8 8 from 0 to 8	
Routing	No	Max. 4

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
Interfaces	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
1st interface		
Type of interface	Integrated RS485 interface	
Physics	RS 485	
electrically isolated	No	
Interface power supply (15 to 30 VDC)	Max. 200 mA	
Functionality		
• MPI	Yes	
• PROFIBUS DP	No	
• Point-to-point connection	No	
MPI		
Number of connections	12	
Services		
• PG/OP communication	Yes	
• Routing	No	Yes
• Global data communication	Yes	
• S7 basic communication	Yes	
• S7 communication – As server – As client	 Yes No (but via CP and loadable FBs)	
• Transmission rates	Max. 187.5 kbps	
2nd interface	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Type of interface	Integrated RS422/RS485 interface	Integrated RS485 interface
Physics	RS 422/485	RS 485
electrically isolated	Yes	Yes
Interface power supply (15 to 30 VDC)	No	Max. 200 mA
Number of connections	None	12
Functionality		
• MPI	No	No
• PROFIBUS DP	No	Yes
• Point-to-point connection	Yes	No
DP master		
Number of connections	–	12
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes
• Global data communication	–	No
• S7 basic communication	–	No
• S7 communication	–	No
• Constant bus cycle time	–	Yes
• SYNC/FREEZE	–	Yes

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
• Enable/disable DP slaves	–	Yes
• DPV1	–	Yes
• Transmission rates	–	Up to 12 Mbaud
• Number of DP slaves per station	–	Max. 32
• Address area	–	Max. 1 KB I / 1 KB O
• User data per DP slave	–	Max. 244 bytes I / 244 bytes O
DP slave		
Number of connections	–	12
Services		
• PG/OP communication	–	Yes
• Routing	–	Yes (only if interface is active)
• Global data communication	–	No
• S7 basic communication	–	No
• S7 communication	–	No
• Direct data exchange	–	Yes
• Transmission rates	–	Up to 12 Mbaud
• Intermediate memory	–	244 bytes I / 244 bytes O
• Automatic baud rate search	–	Yes (only if interface is passive)
• Address areas		Max. 32, with Max. 32 bytes each
• DPV1	–	No
GSD file	–	The latest GSD file is available at: http://www.automation.siemens.com/csi/gsd
Point-to-point connection		
• Transmission rates	38.4 Kbaud half duplex 19.2 Kbaud full duplex	–
• Cable length	Max. 1200 m	–
• User program can control the interface	Yes	–
• The interface can trigger a break or an interrupt in the user program	Yes (message with break ID)	–
• Protocol driver	3964 (R); ASCII and RK512	–
Programming	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Programming language	LAD/FBD/STL	
Available instructions	see the Instruction List	
Nesting levels	8	
System functions (SFCs)	see the Instruction List	
System function blocks (SFBs)	see the Instruction List	
User program security	Yes	

Technical data		
	CPU 314C-2 PtP	**CPU 314C-2 DP**
Integrated I/O	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
• Default addresses of the integrated – Digital inputs – Digital outputs – Analog inputs – Analog outputs	 124.0 to 126.7 124.0 to 125.7 752 to 761 752 to 755	
Integrated functions		
Counters	4 channels (see the Manual *Technological Functions*)	
Frequency counters	4 channels, Max. 60 kHz (see the Manual *Technological Functions*)	
Pulse outputs	4 channels for pulse width modulation, Max. 2.5 kHz (see the Manual *Technological Functions*)	
Controlled positioning	1 channel (see the Manual *Technological Functions*)	
Integrated "Controlling" SFB	PID controller (see the Manual *Technological Functions*)	
Dimensions	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Mounting dimensions W x H x D (mm)	120 x 125 x 130	
Weight	approx. 676 g	
Voltages and currents	**CPU 314C-2 PtP**	**CPU 314C-2 DP**
Power supply (rated value)	24 VDC	
• Permitted range	20.4 V to 28.8 V	
Current consumption (no-load operation)	Typically 150 mA	
Inrush current	Typically 11 A	
Power consumption (nominal value)	800 mA	1000 mA
I^2t	0.7 A^2s	
External fusing of power supply lines (recommended)	LS switch type C min. 2 A, LS switch type B min. 4 A	
Power loss	Typically 14 W	

6.6 Technical data of the integrated I/O

6.6.1 Arrangement and usage of integrated I/Os

Introduction

Integrated I/Os of CPUs 31xC can be used for technological functions or as standard I/O.

The figures below illustrate possible usage of I/Os integrated in the CPUs.

Reference

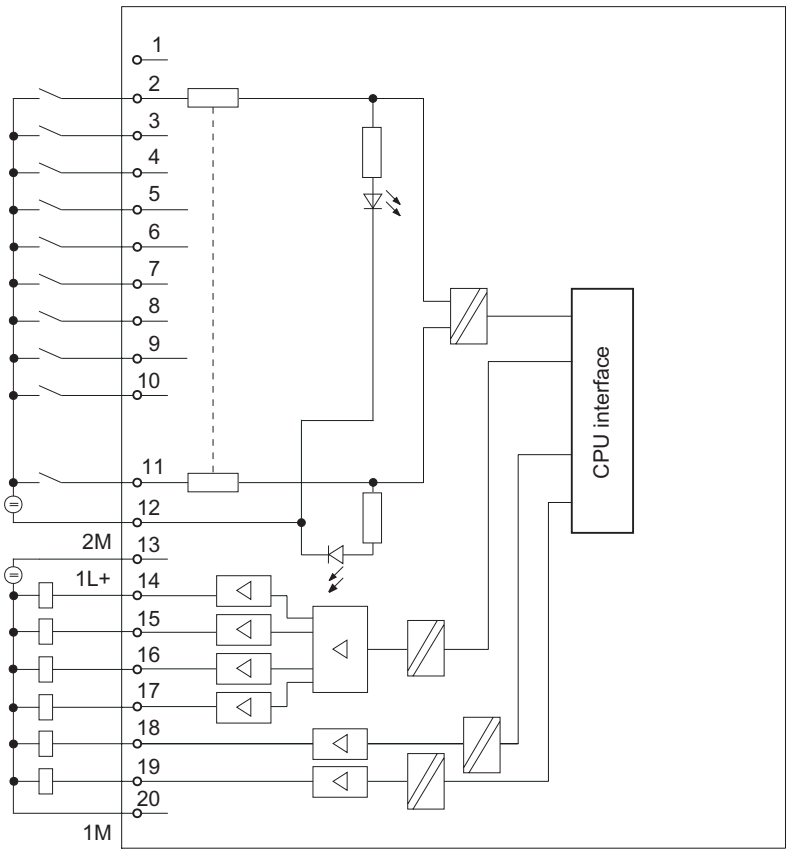
Further information on integrated I/O is found in the Manual *Technical Functions*.

CPU 312C: Pin-out of the integrated DI/DO (connector X11)

Standard	Interrupt input	Count	X11	
			1 ∅	
DI	X	Z0 (A)	2 ∅	DI+0.0
DI	X	Z0 (B)	3 ∅	DI+0.1
DI	X	Z0 (HW-Tor)	4 ∅	DI+0.2
DI	X	Z1 (A)	5 ∅	DI+0.3
DI	X	Z1 (B)	6 ∅	DI+0.4
DI	X	Z1 (HW-Tor)	7 ∅	DI+0.5
DI	X	Latch 0	8 ∅	DI+0.6
DI	X	Latch 1	9 ∅	DI+0.7
DI	X		10 ∅	DI+1.0
DI	X		11 ∅	DI+1.1
			12 ∅	2 M
			13 ∅	1L+
DO		V0	14 ∅	DO+0.0
DO		V1	15 ∅	DO+0.1
DO			16 ∅	DO+0.2
DO			17 ∅	DO+0.3
DO			18 ∅	DO+0.4
DO			19 ∅	DO+0.5
			20 ∅	1 M

Zn	Counter n
A, B	Encoder signas
Vn	Comparator n
X	Pin usable if not assigned to technology functions
HW-Tor	Gate control
Latch	Store counter distance

Block diagram of the integrated digital I/O



CPU 313C, CPU 313C-2 DP/PtP, CPU 314C-2 DP/PtP: DI/DO (connectors X11 and X12)

X11 of CPU 313C-2PtP/DP
X12 of CPU 314C-2PtP/DP

Standard DI	Interrupt input	Count	Positio-ning 1)					Positioning 1) Digital	Positioning 1) Analog	Count	Standard DO
				1 ∅	1L+	2L+	∅ 21				
X	X	Z0 (A)	A 0	2 ∅	DI+0.0	DO+0.0	∅ 22			V0	X
X	X	Z0 (B)	B 0	3 ∅	DI+0.1	DO+0.1	∅ 23			V1	X
X	X	Z0(HW-gate)	N 0	4 ∅	DI+0.2	DO+0.2	∅ 24			V2	X
X	X	Z1 (A)	Tast 0	5 ∅	DI+0.3	DO+0.3	∅ 25			V3 1)	X
X	X	Z1(B)	Bero 0	6 ∅	DI+0.4	DO+0.4	∅ 26				X
X	X	Z1(HW-gate)		7 ∅	DI+0.5	DO+0.5	∅ 27				X
X	X	Z2 (A)		8 ∅	DI+0.6	DO+0.6	∅ 28		CONV_EN		X
X	X	Z2 (B)		9 ∅	DI+0.7	DO+0.7	∅ 29		CONV_DIR		X
				10 ∅		2M	∅ 30				
				11 ∅		3L+	∅ 31				
X	X	Z2 (HW gate)		12 ∅	DI+1.0	DO+1.0	∅ 32	R+			X
X	X	Z3 (A)		13 ∅	DI+1.1	DO+1.1	∅ 33	R-			X
X	X	Z3 (B)	1)	14 ∅	DI+1.2	DO+1.2	∅ 34	Rapid			X
X	X	Z3 (HW gate)		15 ∅	DI+1.3	DO+1.3	∅ 35	Creep			X
X	X	Z0 (Latch)		16 ∅	DI+1.4	DO+1.4	∅ 36				X
X	X	Z1 (Latch)		17 ∅	DI+1.5	DO+1.5	∅ 37				X
X	X	Z2 (Latch)		18 ∅	DI+1.6	DO+1.6	∅ 38				X
X	X	Z3 (Latch)	1)	19 ∅	DI+1.7	DO+1.7	∅ 39				X
				20 ∅	1M	3M	∅ 40				

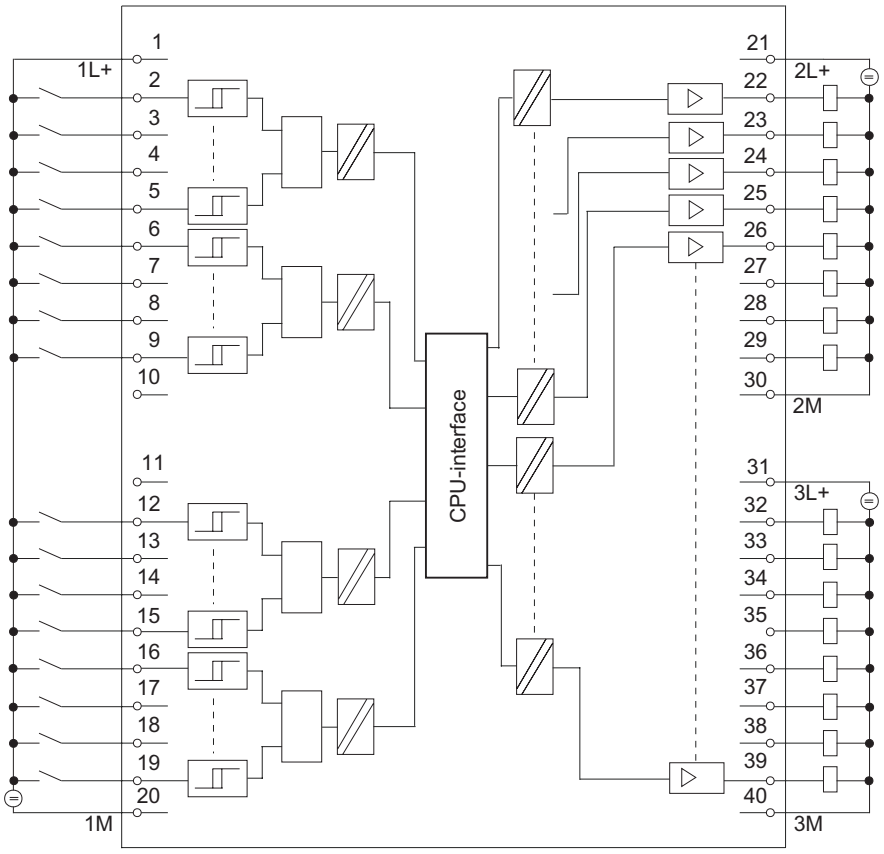
Zn	Counter n
A, B	Encoder signals
HW gate	Gate control
Latch	Store counter distance
Vn	Comparator n
Prob 0	Measuring probe 0
Bero 0	Reference point switch 0
R+, R-	Directional signal
Rapid	Rapid traverse
Creep	Creep speed
CONV_EN	Power section enable
CONV_DIR	Directional signal (only with control type "voltage 0 to 10 V or current from 0 to 10 mA and directional signal")
X	Pin usable if not assigned to technology functions

1) CPU 314C-2 only

Reference

Details are found in the Manual *Technical Functions* under *Counting, Frequency Measurement and Pulse Width Modulation*

Block diagram of integrated digital I/O of CPUs 313C/313C-2/314C-2



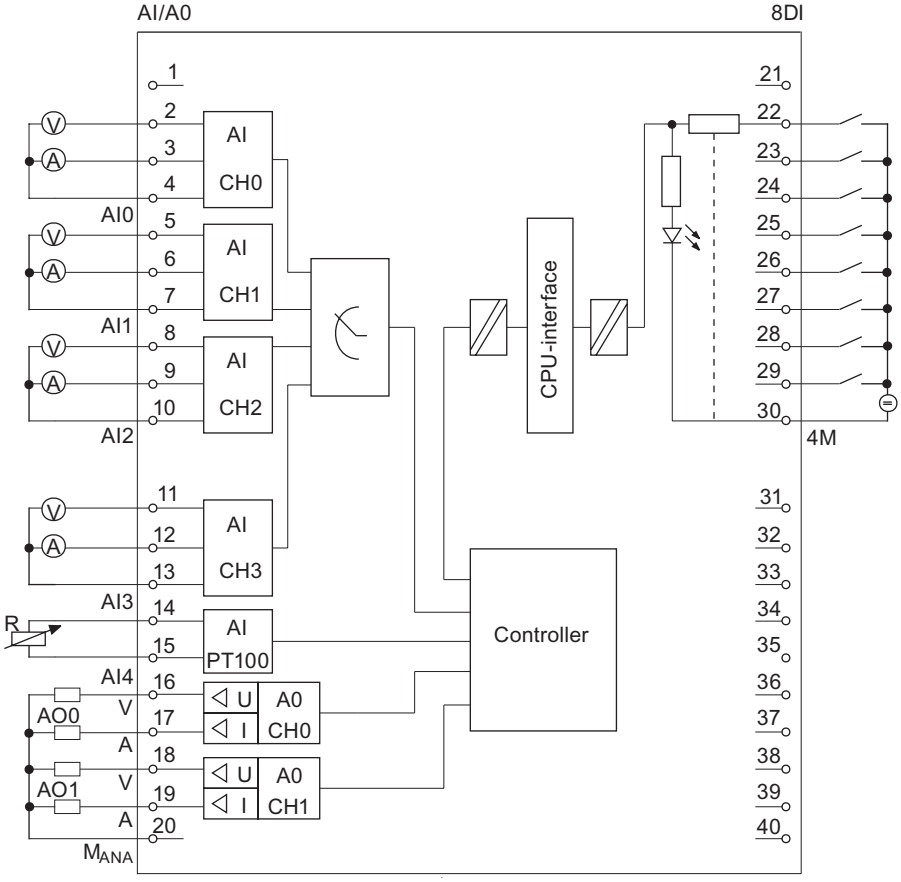
CPU 313C/314C-2: Pin-out of the integrated AI/AO and DI (connector X11)

X11

Standard		Positioning[1]	1			∅ 21	Standard-DI	Interrupt input
AI (Ch0)	V		2 ∅	PEWx+0	DI+2.0	∅ 22	X	X
	I		3 ∅		DI+2.1	∅ 23	X	X
	C		4 ∅		DI+2.2	∅ 24	X	X
AI (Ch1)	V		5 ∅	PEWx+2	DI+2.3	∅ 25	X	X
	I		6 ∅		DI+2.4	∅ 26	X	X
	C		7 ∅		DI+2.5	∅ 27	X	X
AI (Ch2)	V		8 ∅	PEWx+4	DI+2.6	∅ 28	X	X
	I		9 ∅		DI+2.7	∅ 29	X	X
	C		10 ∅		4M	∅ 30		
AI (Ch3)	V		11 ∅	PEWx+6		∅ 31		
	I		12 ∅			∅ 32		
	C		13 ∅			∅ 33		
PT 100 (Ch4)			14 ∅	PEWx+8		∅ 34		
			15 ∅			∅ 35		
AO (Ch0)	V	Control-output 0	16 ∅	PEWx+0		∅ 36		
	A		17 ∅			∅ 37		
AO (Ch1)	V		18 ∅	PEWx+8		∅ 38		
	A		19 ∅			∅ 39		
			20 ∅	M_{ANA}		∅ 40		

1) CPU 314C-2 only

Block diagram of integrated digital/analog I/O of CPUs 313C/314C-2



Simultaneous usage of technological functions and standard I/O

Technological functions and standard I/O can be used simultaneously with appropriate hardware. For example, you can use all digital inputs not used for counting functions as standard DI.

Read access to inputs used by technological functions is possible. Write access to outputs used by technological functions is not possible.

See also

CPU 312C (Page 6-3)

CPU 313C (Page 6-8)

CPU 313C-2 PtP and CPU 313C-2 DP (Page 6-14)

CPU 314C-2 PtP and CPU 314C-2 DP (Page 6-21)

6.6.2 Analog I/O

Wiring of the current/voltage inputs

The figure below shows the wiring diagram of the current/voltage inputs operated with 2-/4-wire measuring transducers.

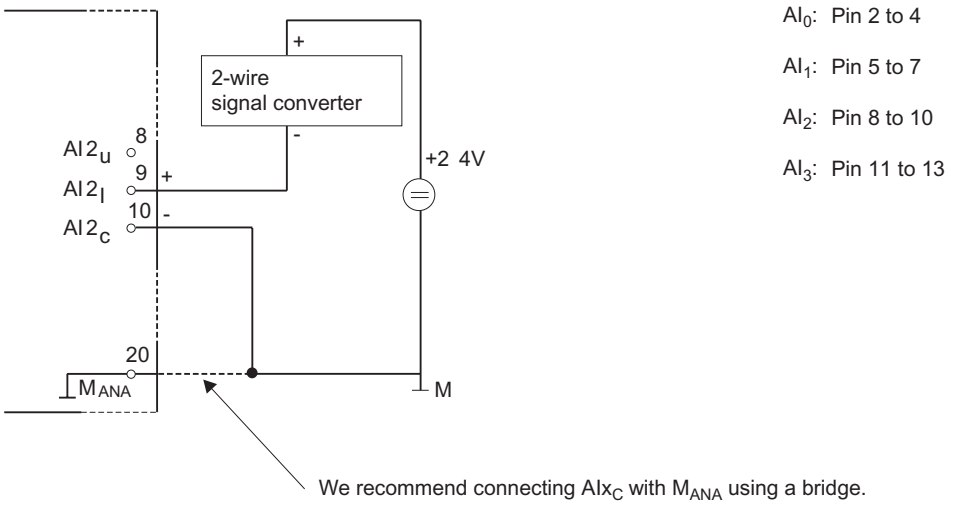


Figure 6-1 Connection of a 2-wire measuring transducer to an analog current/voltage input of CPU 313C/314C-2

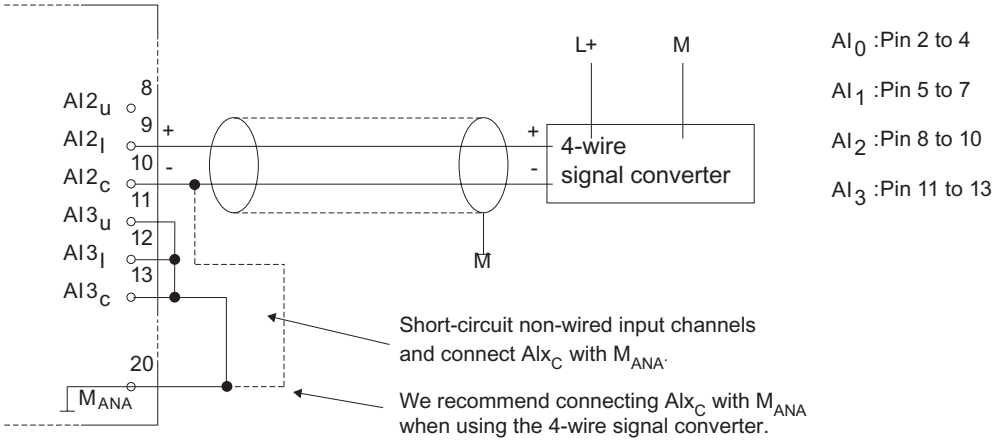


Figure 6-2 Connection of a 4-wire measuring transducer to an analog current/voltage input of CPU 313C/314C-2

Measurement principle

31xC CPUs use the measurement principle of actual value encoding. Here, they operate with a sampling rate of 1 kHz. That is, a new value is available at the peripheral input word register once every millisecond. This value can then be read via user program (e.g. L PEW). The "previous" value is read again if access times are shorter than 1 ms.

Integrated hardware low-pass filter

An integrated low-pass filter attenuates analog input signals of channel 0 to 3. They are attenuated according to the trend in the figure below.

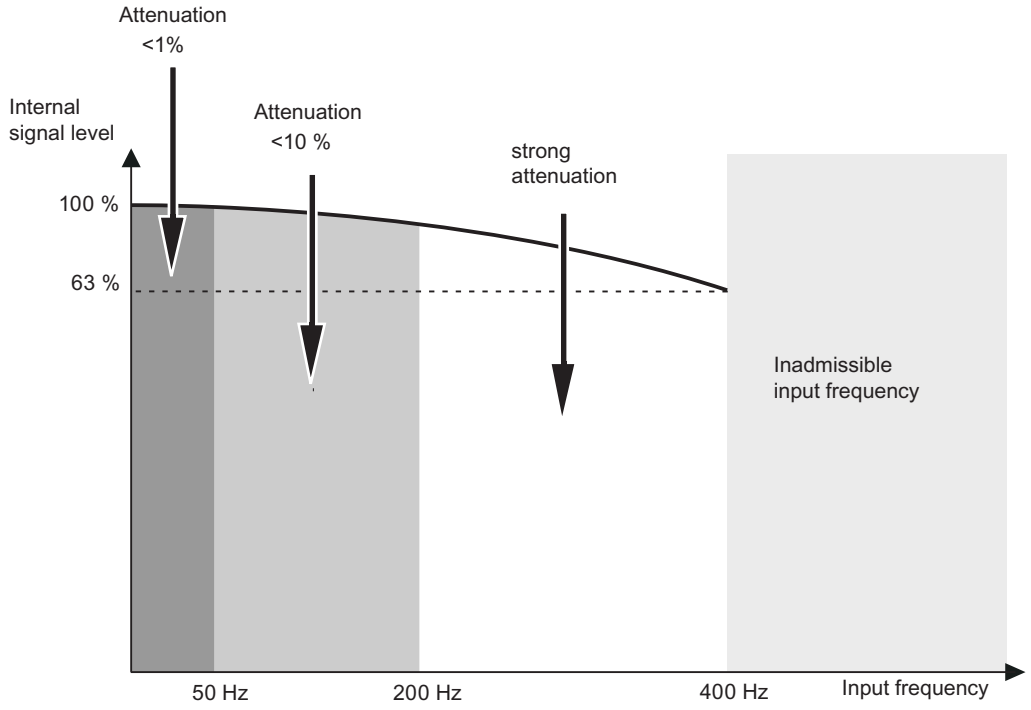


Figure 6-3 Low-pass characteristics of the integrated filter

Note

The maximum frequency of the input signal is 400 Hz.

Input filters (software filter)

The current / voltage inputs have a software filter for the input signals which can be programmed with STEP 7. It filters the configured interference frequency (50/60 Hz) and multiples thereof.

The selected interference suppression also determines the integration time.
At an interference suppression of 50 Hz the software filter forms the average based on the last 20 measurements and saves the result as a measurement value.

You can suppress interference frequencies (50 Hz or 60 Hz) according to the parameters set in STEP 7. A setting of 400 Hz will not suppress interference.

An integrated low-pass filter attenuates analog input signals of channel 0 to 3.

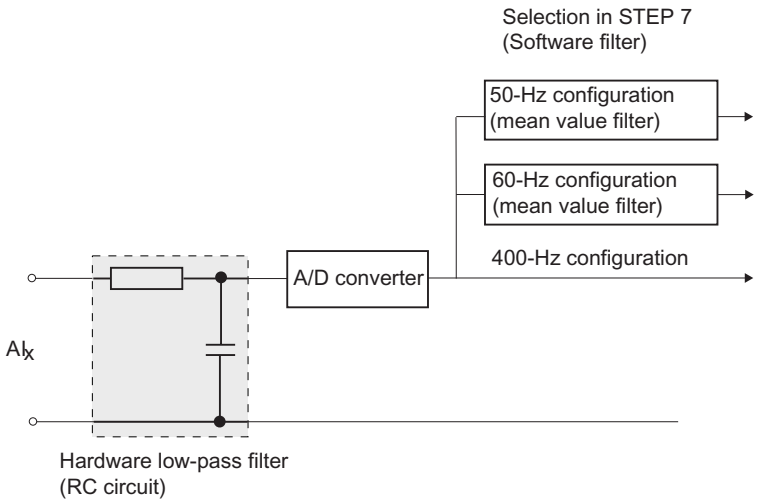


Figure 6-4 Principle of interference suppression with STEP 7

In the two graphics below we illustrate how the 50 Hz and 60 Hz interference suppression work

Example of a 50-Hz parasitic frequency suppression (integration time corresponds to 20 ms)

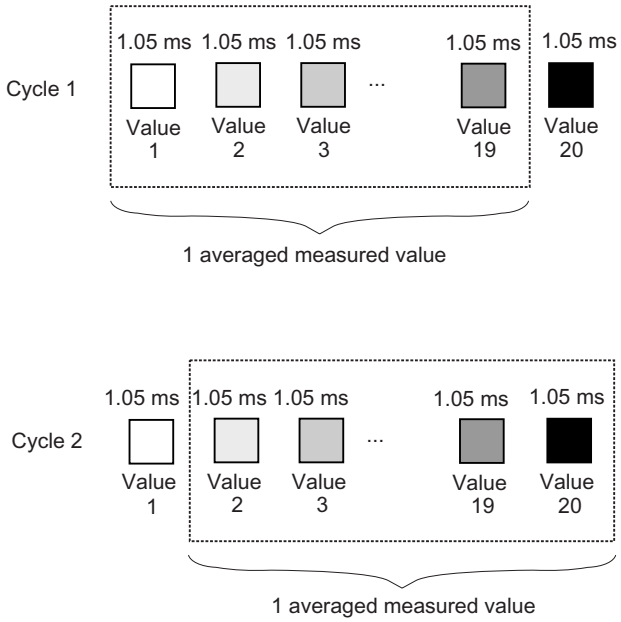


Figure 6-5 50 Hz interference suppression

Example of a 60-Hz parasitic frequency suppression (integration time corresponds to 16,7 ms)

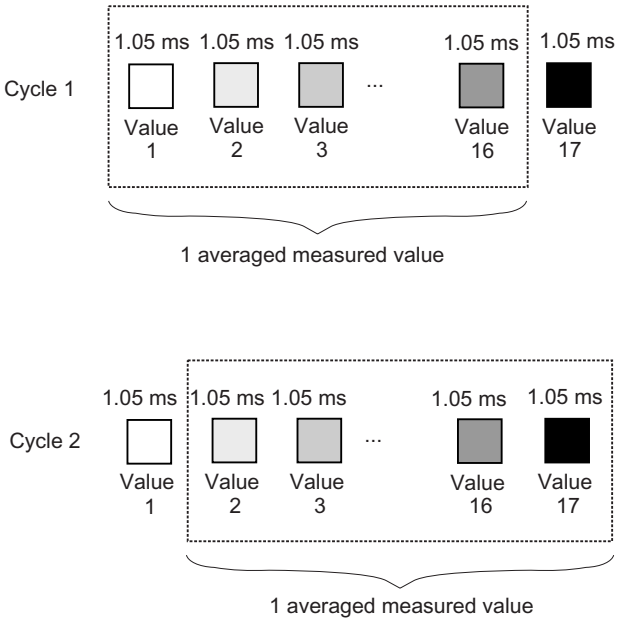


Figure 6-6 60 Hz interference suppression

Note

If the interference frequency is not 50/60 Hz or a multiple thereof, the input signal must be filtered externally,
In this case, 400 Hz frequency suppression must be configured for the respective input. This is equivalent to a "Deactivation" of the software filter.

Inputs not connected

The three inputs of a current/voltage analog output channel that is not connected should be bypasses and connected to M_{ANA} (pin 20 of the front connector). This ensures maximum interference resistance for these analog inputs.

Outputs not connected

In order to disconnect unused analog outputs from power, you must disable and leave them open during parameter assignment with STEP 7.

Reference

Details (visualization and processing of analog values, for example) are found in chapter 4 of the *Module Data* Reference Manual.

6.6.3 Parameterization

Introduction

You configure the integrated I/O of CPU 31xC with STEP 7. Always make these settings when the CPU is in STOP. The generated parameters are downloaded from the PG to the S7-300 and written to CPU memory .

You can also choose to change the parameters at SFC 55 in the user program (see the Reference Manual *System and Standard Functions*). Refer to the structure of record 1 for the respective parameters.

Parameters of standard DI

The table below gives you an overview of the parameters for standard digital inputs.

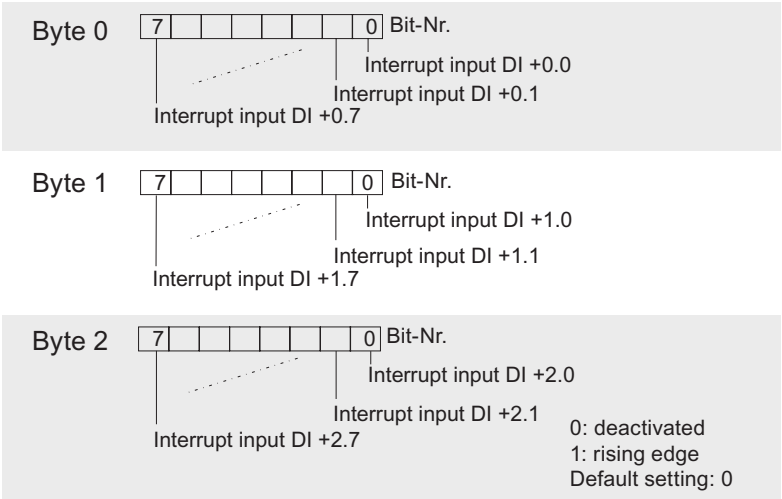
Table 6-7 Parameters of standard DI

Parameters	Value range	Default	Range of efficiency
Input delay (ms)	0,1/0,5/3/15	3	Channel group

The table below gives you an overview of the parameters when using digital inputs as interrupt inputs.

Table 6-8 Parameters of the interrupt inputs

Parameters	Value range	Default	Range of efficiency
Interrupt input	Disabled / positive edge	De-activated	digital input
Interrupt input	Disabled/ negative edge	De-activated	digital input



Byte 3 reserverd

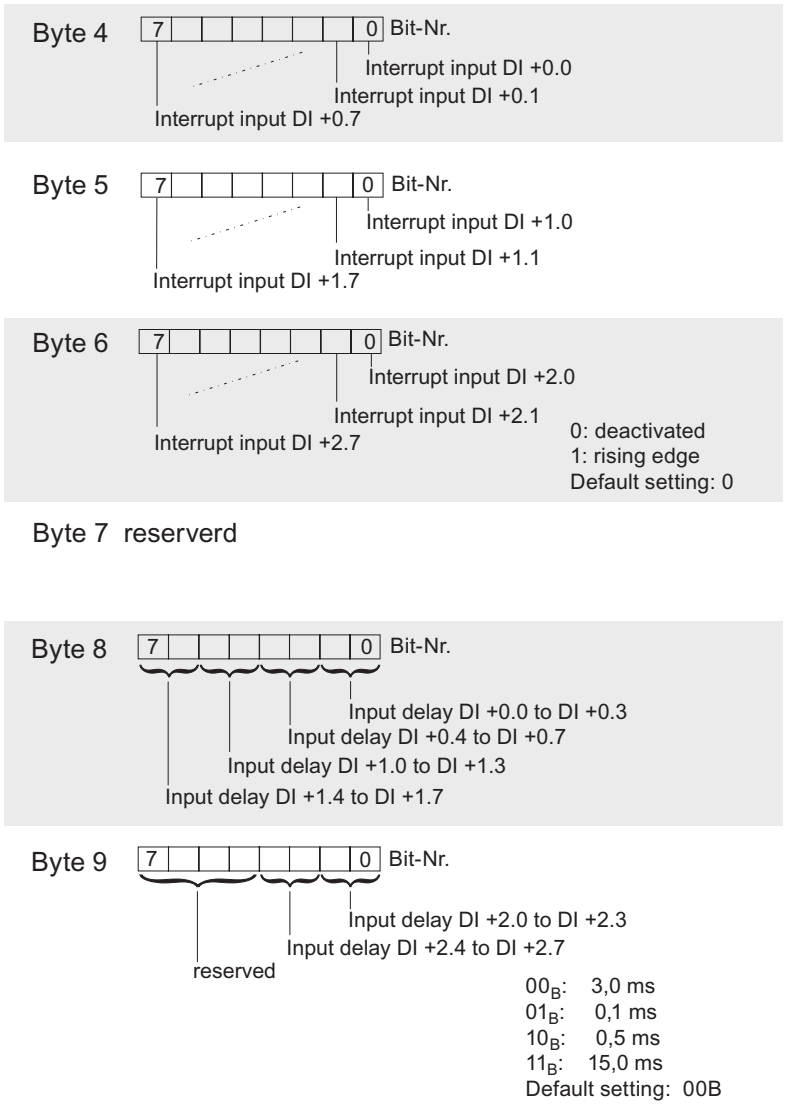


Figure 6-7 Structure of record 1 for standard DI and interrupt inputs (length of 10 bytes)

Parameters of standard DO

There are no parameters for standard digital outputs.

Parameters of standard AI

The table below gives you an overview of the parameters for standard analog inputs.

Table 6-9 Parameters of standard AI

Parameters	Value range	Default	Range of efficiency
Integration time (ms) Interference suppression (Hz) (channel 0 to 3)	2,5/16,6/20 400/60/50	20 50	Channel Channel
Measurement range (channel 0 to 3)	deactivated/ +/- 20 mA/ 0 ... 20 mA/ 4 ... 20 mA/ +/- 10 V/ 0 ... 10 V	+/- 10 V	Channel
Type of measurement (channel 0 to 3)	deactivated/ U voltage/ I current	U voltage	Channel
Unit of measurement (channel 4)	Celsius/Fahrenheit/ Kelvin	Celsius	Channel
Measurement range (Pt 100 input; channel 4)	deactivated/ Pt 100/600 Ω	600 Ω	Channel
Type of measurement (Pt 100 input; channel 4)	deactivated/ Resistance/ Thermal resistance	Resistance	Channel

Reference

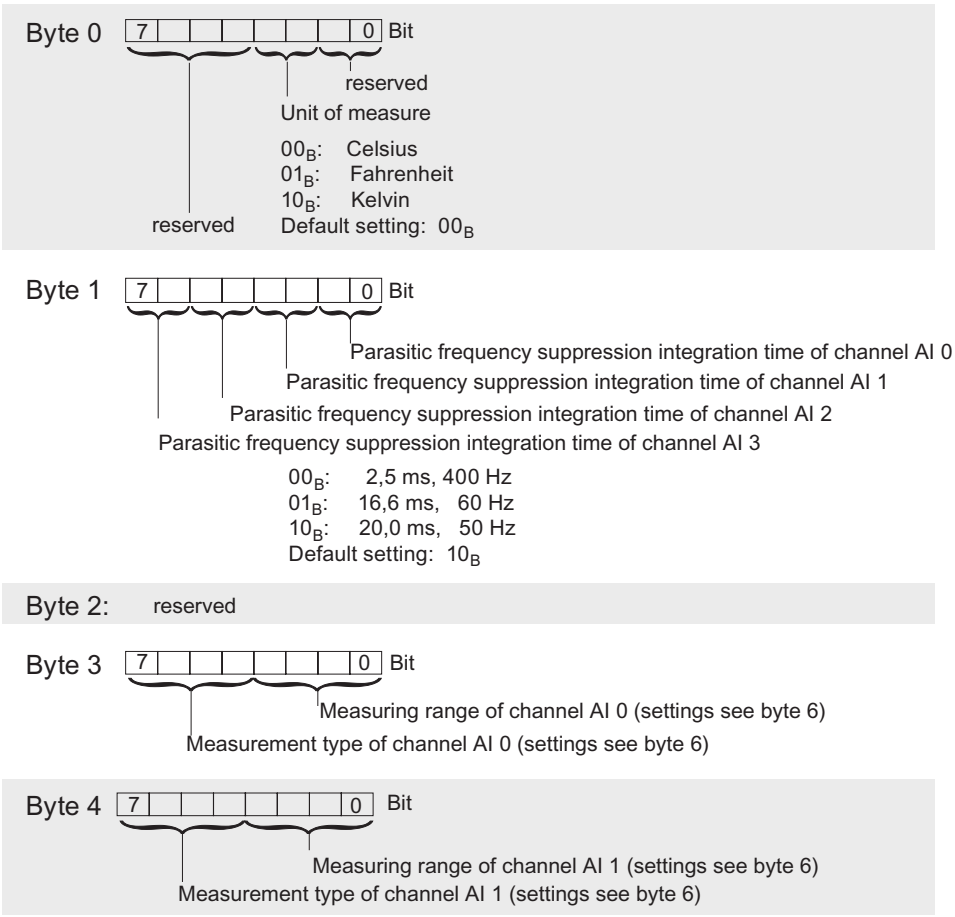
See also Chapter 4.3 in the *Module Data* Reference Manual.

Parameters of standard AO

The table below gives you an overview of standard analog output parameters (see also Chapter 4.3 in the *Module Data* Reference Manual).

Table 6-10 Parameters of standard AO

Parameters	Value range	Default	Range of efficiency
Output range (channel 0 to 1)	deactivated/ +/- 20 mA/ 0 ... 20 mA/ 4 ... 20 mA/ +/- 10 V/ 0 ... 10 V	+/- 10 V	Channel
Type of output (channel 0 to 1)	deactivated/ U voltage/ I current	U voltage	Channel


Byte 0
7
0
Bit
reserved
Unit of measure
00B: Celsius
01B: Fahrenheit
10B: Kelvin
reserved
Default setting: 00B
Byte 1
7
0
Bit
Parasitic frequency suppression integration time of channel AI 0
Parasitic frequency suppression integration time of channel AI 1
Parasitic frequency suppression integration time of channel AI 2
Parasitic frequency suppression integration time of channel AI 3
00B: 2,5 ms, 400 Hz
01B: 16,6 ms, 60 Hz
10B: 20,0 ms, 50 Hz
Default setting: 10B
Byte 2: reserved
Byte 3
7
0
Bit
Measuring range of channel AI 0 (settings see byte 6)
Measurement type of channel AI 0 (settings see byte 6)
Byte 4
7
0
Bit
Measuring range of channel AI 1 (settings see byte 6)
Measurement type of channel AI 1 (settings see byte 6)

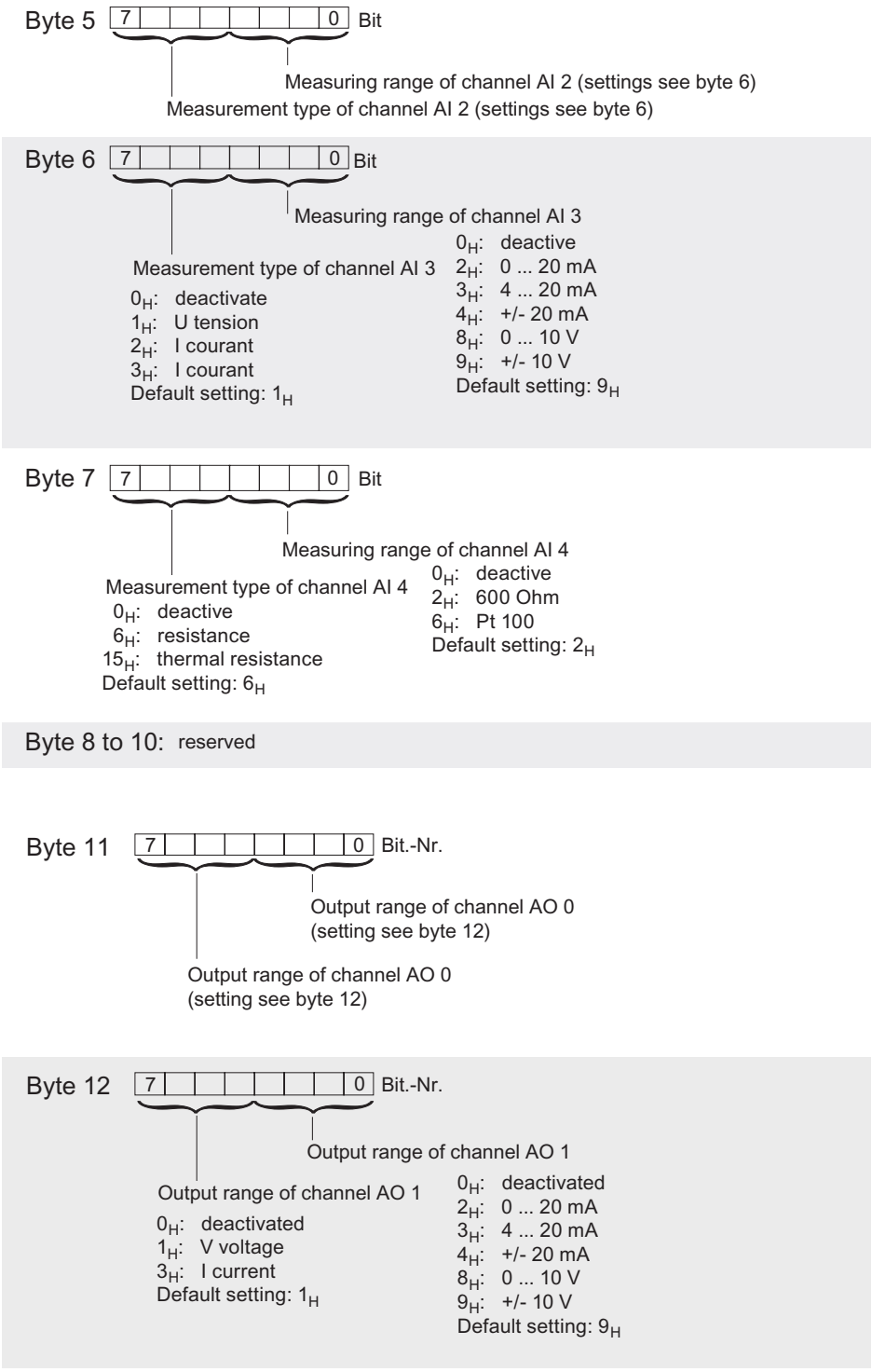


Figure 6-8 Structure of record 1 for standard AI/AO (length of 13 bytes)

Parameter for technological functions

The parameters for the respective function are found in the Manual *Technological Functions*.

6.6.4 Interrupts

Interrupt inputs

All digital inputs of the on-board I/O of CPUs 31xC can be used as interrupt inputs.

You can specify interrupt behavior for each individual input in your parameter declaration. Options are:

- no interrupt
- Interrupt at the positive edge
- Interrupt at the negative edge
- Interrupt at the positive and negative edge

Note

Every channel will hold one event if the rate of incoming interrupts exceeds the handling capacity of OB40. Further events (interrupts) will be lost, without diagnostics or explicit message.

Start information for OB40

The table below shows the relevant temporary variables (TEMP) of OB40 for the interrupt inputs of 31xC CPUs. A description of process interrupt OB 40 is found in the Reference Manual *System and Standard Functions*.

Table 6-11 Start information for OB40, relating to the interrupt inputs of the integrated I/O

Byte	Variables	Data type		Description
6/7	OB40_MDL_ADDR	WORD	B#16#7C	Address of the interrupt-triggering module (here: default addresses of the digital inputs)
8 on	OB40_POINT_ADDR	DWORD	see the figure below	Displaying the interrupt-triggering integrated inputs

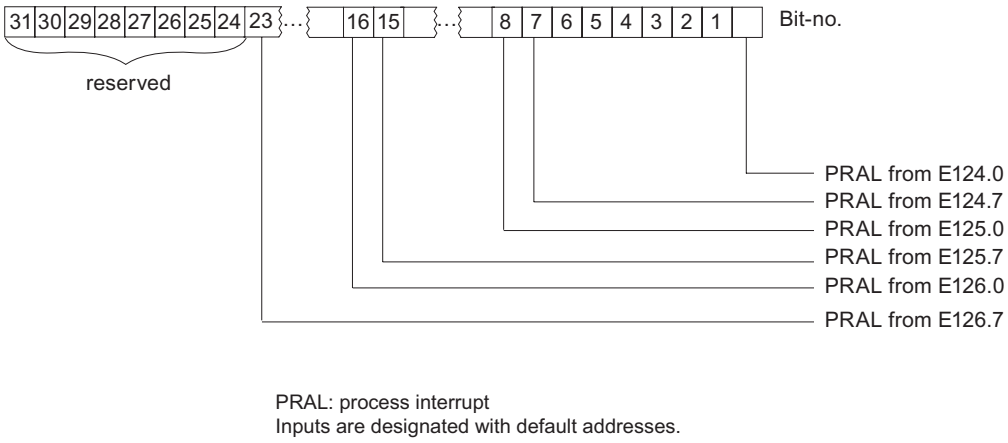


Figure 6-9 Displaying the statuses of CPU 31xC interrupt inputs

PRAL: process interrupt

The inputs are assigned default addresses.

6.6.5 Diagnostics

Standard I/O

Diagnostic data is not available for integrated I/O which is operated as standard I/O (see also the Reference Manual *Module Data*).

Technological functions

Diagnostics options for the respective technological function are found in the Manual *Technological Functions*.

6.6.6 Digital inputs

Introduction

This section provides the specifications for the digital inputs of CPUs 31xC.

The table includes the following CPUs:

- under CPU 313C-2, the CPU 313C-2 DP and CPU 313C-2 PtP
- under CPU 314C-2, the CPU 314C-2 DP and CPU 314C-2 PtP

Technical data

Table 6-12 Technical data of digital inputs

Technical data				
	CPU 312C	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Module-specific data	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Number of inputs	10	24	16	24
• Number of these inputs which can be used for technological functions	8	12	12	16
Cable length				
• Unshielded	For standard DI: Max. 600 m For technological functions: No			
• Shielded	For standard DI: Max. 1000 m			
	For technological function at Max. counting frequency			
	100 m	100 m	100 m	50 m
Voltage, currents, potentials	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Rated load voltage L+	DC 24 V			
• Polarity reversal protection	Yes			
Number of inputs which can be controlled simultaneously				
• Horizontal assembly – Up to 40 °C – up to 60 °C	 10 5	 24 12	 16 8	 24 12
• Vertical assembly – Up to 40 °C	 5	 12	 8	 12
Electrical isolation				
• Between channels and the backplane bus	Yes			
• Between the channels	No			
Permitted potential difference				
• Between different circuits	75 VDC / 60 VAC			
Insulation test voltage	500 VDC			
Current consumption				
• On load voltage L+ (no-load)	–	Max. 70 mA	Max. 70 mA	Max. 70 mA

Technical data				
	CPU 312C	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Status, interrupts, diagnostics	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Status display	green LED per channel			
Interrupts	• Yes, if the corresponding channel is configured as interrupt input • For using technological functions, please refer to the *Technological Functions* Manual.			
Diagnostics functions	• no diagnostics when operated as standard I/O • For using technological functions, please refer to the *Technological Functions* Manual.			
Data for the selection of an encoder for standard DI	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Input voltage				
• Rated value	DC 24 V			
• For signal "1"	15 V to 30 V			
• For signal "0"	-3 V to 5 V			
Input current				
• For signal "1"	Typically 9 mA			
Delay of standard inputs				
• Configurable	Yes (0.1 / 0.5 / 3 / 15 ms) You can reconfigure the input delay of the standard inputs during program runtime. Please note that your newly set filter time may only take effect after the previously set filter time has expired.			
• Rated value	3 ms			
For using technological functions: "Minimum pulse width/ minimum pause between pulses at maximum counting frequency"	48 µs	16 µs	16 µs	8 µs
Input characteristics curve	to IEC 1131, type 1			
Connection of 2wire BEROs	Possible			
• Permitted quiescent current	Max. 1,5 mA			

6.6.7 Digital outputs

Introduction

This chapter contains the specifications for the digital outputs of CPUs 31xC.

The table includes the following CPUs:

- under CPU 313C-2, the CPU 313C-2 DP and CPU 313C-2 PtP
- under CPU 314C-2, the CPU 314C-2 DP and CPU 314C-2 PtP

Fast digital outputs

Technological functions use fast digital outputs.

Technical data

Table 6-13 Technical data of digital outputs

Technical data				
	CPU 312C	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Module-specific data	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Number of outputs	6	16	16	16
• Of those are fast outputs	2	4	4	4
	Caution: You cannot connect the high-speed outputs of your CPU in parallel.			
Cable length				
• Unshielded	Max. 600 m			
• Shielded	Max. 1000 m			
Voltage, currents, potentials	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Rated load voltage L+	24 VDC			
• Polarity reversal protection	No			
Total current of outputs (per group)				
• Horizontal assembly				
– Up to 40° C	Max. 2,0 A	Max. 3,0 A	Max. 3,0 A	Max. 3,0 A
– up to 60 °C	Max. 1,5 A	Max. 2,0 A	Max. 2,0 A	Max. 2,0 A
• Vertical assembly				
– Up to 40° C	Max. 1,5 A	Max. 2,0 A	Max. 2,0 A	Max. 2,0 A
Electrical isolation				
• Between channels and the backplane bus	Yes			
• Between the channels	No	Yes	Yes	Yes
– In groups of	–	8	8	8
Permitted potential difference				
• Between different circuits	75 VDC / 60 VAC			
Insulation test voltage	500 VDC			

Technical data				
	CPU 312C	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Current consumption				
• with load voltage L+	Max. 50 mA	Max. 100 mA	Max. 100 mA	Max. 100 mA
Status, interrupts, diagnostics	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Status display	green LED per channel			
Interrupts	• no interrupts when operated as standard I/O • For using technological functions, please refer to the *Technological Functions* Manual.			
Diagnostics functions	• no diagnostics when operated as standard I/O • For using technological functions, please refer to the *Technological Functions* Manual.			
Data for the selection of an actuator for standard DI	**CPU 312C**	**CPU 313C**	**CPU 313C-2**	**CPU 314C-2**
Output voltage				
• For signal "1"	Min. L+ (-0.8 V)			
Output current				
• For signal "1" – Rated value – Permitted range	0,5 A 5 mA to 600 mA			
• For signal "0" (residual current)	Max. 0.5 mA			
Load impedance range	48 Ω to 4 kΩ			
Lamp load	Max. 5 W			
Parallel connection of 2 outputs				
• for redundant load control	Supported			
• for performance increase	Not possible			
Controlling of digital inputs	Supported			
Switching frequency				
• under resistive load	Max. 100 Hz			
• For inductive load to IEC 947-5, DC13	Max. 0.5 Hz			
• under lamp load	Max. 100 Hz			
• fast outputs under resistive load	Max. 2.5 kHz			
Inductive breaking voltage limited internally to	Typically (L+) - 48 V			
Short-circuit protection of the output	Yes, electronic			
• Response threshold	Typically 1 A			

6.6.8 Analog inputs

Introduction

This chapter contains the specifications for analog outputs of CPUs 31xC.

The table includes the following CPUs:

- CPU 313C
- CPU 314C-2 DP
- CPU 314C-2 PtP

Technical data

Table 6-14 Technical data of analog inputs

Technical data	
Module-specific data	
Number of inputs	4 channels with current/voltage input 1 channel with resistance input
Cable length	
• Shielded	Max. 100 m
Voltage, currents, potentials	
Resistance input	
• No-load voltage	Typically 2.5 V
• Measurement current	Typically 1.8 mA to 3.3 mA
Electrical isolation	
• Between channels and the backplane bus	Yes
• Between the channels	No
Permitted potential difference	
• Between inputs (AI_C) and M_{ANA} (U_{CM})	8.0 VDC
• between M_{ANA} and $M_{internal}$ (U_{ISO})	75 VDC / 60 VAC
Insulation test voltage	600 VDC
Analog value generation	
Measurement principle	Actual value encoding (successive approximation)
Integration time/conversion time/resolution (per channel)	
• Configurable	Yes
• Integration time in ms	2,5 / 16,6 / 20
• Permitted input frequency	Max. 400 Hz
• Resolution (including overdrive)	11 bits + signed bit
• Suppression of interference frequency f1	400 / 60 / 50 Hz
Time constant of the input filter	0,38 ms
Basic processing time	1 ms

Technical data	
Interference suppression, error limits	
Interference voltage suppression for f = nx (f1 ± 1 %), (f1 = interference frequency), n = 1, 2	
• Commonmode interference (U_{CM} < 1.0 V)	> 40 dB
• Feedback interference (peak value of the interference < rated value of the input range)	> 30 dB
Crosstalk between the inputs	> 60 dB
Operational error limits (across the temperature range, in relation to input range)	
• Voltage/current	< 1 %
• Resistance	< 5 %
Basic error limit (operational limit at 25 °C, in relation to input range)	
• Voltage/current – Linearity error during measurement of current and voltage (related to input range)	< 0,7 % ± 0,06 %
• Existence – Linearity error during resistance measurement (related to input range)	< 3 % ± 0,2 %
Temperature error (in relation to input range)	± 0,006 %/K
Repeat accuracy (in transient state at 25 °C, in relation to input range)	± 0,06 %
Status, interrupts, diagnostics	
Interrupts	• no interrupts when operated as standard I/O
Diagnostics functions	• no diagnostics when operated as standard I/O • For using technological functions, please refer to the *Technological Functions* Manual.
Encoder selection data	
Input ranges (rated value)/input resistance	
• Voltage	± 10 V/100 kΩ 0 V to 10 V/100 kΩ
• Current	± 20 mA/50 Ω 0 mA to 20 mA/50 Ω 4 mA to 20 mA/50 Ω
• Existence	0 Ω to 600 Ω/10 MΩ
• Resistance thermometer	Pt 100/10 MΩ
Permitted continuous input voltage (destruction limit)	
• For voltage inputs	Max. 30 V
• For current inputs	Max. 2.5 V
Permitted continuous input current (destruction limit)	
• For voltage inputs	Max. 0,5 mA;
• For current inputs	Max. 50 mA;

Technical data	
Connection of signal generators	
• For voltage measurement	possible
• For current measurement – as 2-wire measuring transducer – as 4-wire measuring transducer	 Possible, with external power supply possible
• for measuring resistance – with 2-conductor terminal – with 3-wire connection – with 4-wire connection	 Possible, without compensation of cable resistance Not possible Not possible
Linearization of the characteristics trend	By software
• For resistance thermometers	Pt 100
Temperature compensation	No
Technical unit for temperature measurement	Degrees Celsius/Fahrenheit/Kelvin

6.6.9 Analog outputs

Introduction

This chapter contains the specifications for digital outputs of CPUs 31xC.

The table includes the following CPUs:

- CPU 313C
- CPU 314C-2 DP
- CPU 314C-2 PtP

Technical data

Table 6-15 Technical data of analog outputs

Technical data	
Module-specific data	
Number of outputs	2
Cable length	
• Shielded	Max. 200 m
Voltage, currents, potentials	
Rated load voltage L+	24 VDC
• Polarity reversal protection	Yes
Electrical isolation	
• Between channels and the backplane bus	Yes
• Between the channels	No

Technical data	
Permitted potential difference	
• between M_{ANA} and $M_{internal}$ (U_{ISO})	75 VDC / 60 VAC
Insulation test voltage	600 VDC
Analog value generation	
Resolution (including overdrive)	11 bits + signed bit
Conversion time (per channel)	1 ms
Settling time	
• with resistive load	0,6 ms
• With capacitive load	1,0 ms
• With inductive load	0.5 ms
Interference suppression, error limits	
Crosstalk between the outputs	> 60 dB
Operational error limits (across the temperature range, in relation to output range)	
• Voltage/current	± 1 %
Basic error limit (operational limit at 25 °C, in relation to output range)	
• Voltage/current	± 0,7 %
Temperature error (in relation to output range)	± 0.01 %/K
Linearity error (in relation to output range)	± 0,15 %
Repeat accuracy (in transient state at 25 °C, in relation to output range)	± 0,06 %
Output ripple; bandwidth 0 to 50 kHz (in relation to output range)	± 0,1 %
Status, interrupts, diagnostics	
Interrupts	• no interrupts when operated as standard I/O • For using technological functions, please refer to the *Technological Functions* Manual.
Diagnostics functions	• no diagnostics when operated as standard I/O • For using technological functions, please refer to the *Technological Functions* Manual.
Actuator selection data	
Output range (rated values)	
• Voltage	± 10 V 0 V to 10 V
• Current	± 20 mA 0 mA to 20 mA 4 mA to 20 mA
Load resistance (within output rating)	
• For voltage outputs – Capacitive load	Min. 1 kΩ Max. 0.1 µF
• For current outputs – Inductive load	Max. 300 Ω 0.1 mH

Technical data	
Voltage output	
• Short-circuit protection	Yes
• Short-circuit current	Typically 55 mA
Current output	
• No-load voltage	Typically 17 V
Destruction limit for externally applied voltages/currents	
• Voltage measured between the outputs and M_{ANA}	Max. 16 V
• Current	Max. 50 mA;
Connection of actuators	
• For voltage outputs – wire connection – wire connection (test lead)	 Possible, without compensation of cable resistance Not possible
• For current outputs – wire connection	 Possible

Technical data of CPU 31x

7

7.1 General technical data

7.1.1 Dimensions of CPU 31x

Each CPU features the same height and depth, only the width dimensions differ.

- Height: 125 mm
- Depth: 115 mm, or 180 mm with opened front cover.

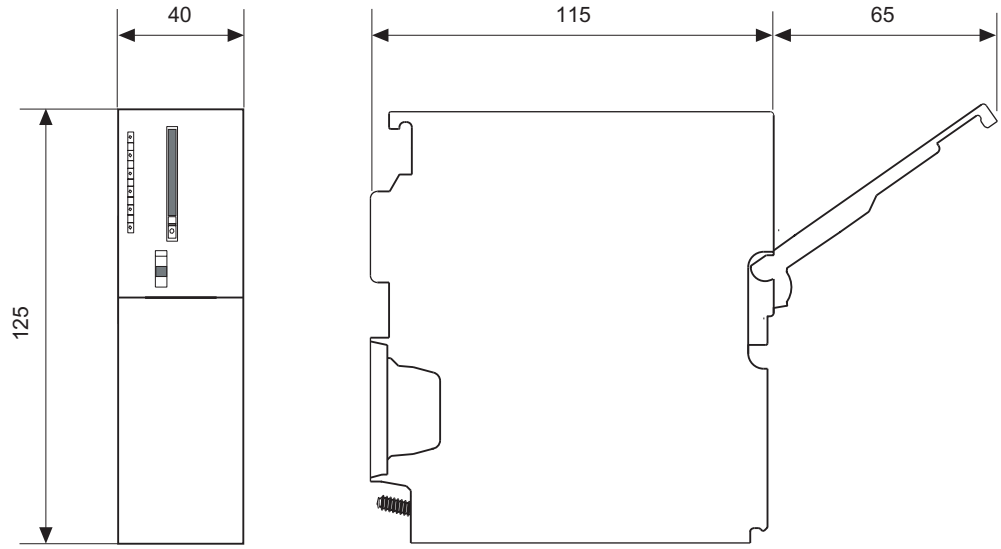


Figure 7-1 Dimensions of CPU 31x

Width of CPU

CPU	Width
CPU 312	40 mm
CPU 314	40 mm
CPU 315-2 DP	40 mm
CPU 315-2 PN/DP	80 mm
CPU 317-2 DP	80 mm
CPU 317-2 PN/DP	80 mm
CPU 319	120 mm

7.1.2 Technical specifications of the SIMATIC Micro Memory Card (MMC)

Plug-in SIMATIC Micro Memory Card (MMC)

The following memory modules are available:

Table 7-1 Available SIMATIC Micro Memory Cards

Type	Order number	Required for a firmware update via SIMATIC Micro Memory Card
MMC 64k	6ES7 953-8LFxx-0AA0	–
MMC 128k	6ES7 953-8LGxx-0AA0	–
MMC 512k	6ES7 953-8LJxx-0AA0	–
MMC 2M	6ES7 953-8LLxx-0AA0	Minimum requirement for CPUs without DP interface
MMC 4M	6ES7 953-8LMxx-0AA0	Minimum requirement for CPUs without DP interface (except CPU 319)
MMC 8M [1]	6ES7 953-8LPxx-0AA0	Minimum requirements for the CPU 319

[1] If you plug in the CPU 312C or CPU 312, you cannot use this SIMATIC Micro Memory Card.

Maximum number of loadable blocks on the SIMATIC Micro Memory Card

Number of blocks that can be stored on the SIMATIC Micro Memory Card depends on the capacity of the SIMATIC Micro Memory Card being used The maximum number of blocks that can be loaded is therefore limited by the capacity of your MMC (including blocks generated with the "CREATE DB" SFC)

Table 7-2 Maximum number of loadable blocks on the SIMATIC Micro Memory Card

Size of SIMATIC Micro Memory Card	Maximum number of blocks that can be loaded
64 KB	768
128 KB	1024
512 KB	Here the maximum number of blocks that can be loaded for the specific CPU is less than the number of blocks that can be stored on the SIMATIC Micro Memory Card. Refer to the corresponding specifications of a specific CPU to determine the maximum number of blocks that can be loaded.
2 MB	
4 MB	
8 MB	

7.2 CPU 312

Technical data

Table 7-3 Technical data for the CPU 312

Technical data	
CPU and version	
Order no. [MLFB]	6ES7312-1AD10-0AB0
• Hardware version	01
• Firmware version	V2.0.0
• Associated programming package	STEP 7 as of V 5.1 + SP 4
Memory	
Work memory	
• Integrated	16 Kbytes
• Expandable	No
Load memory	Plugged in with MMC (Max. 4 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	Guaranteed by MMC (maintenance-free)
Execution times	
Processing times of	
• Bit instructions	Min. 0.2 µs
• Word instructions	Min. 0.4 µs
• Fixed-point arithmetic	Min. 5 µs
• Floating-point maths	Min. 6 µs
Timers/counters and their retentive address areas	
S7 counters	128
• Retentive address areas	Configurable
• Default	From C0 to C7
• Counting range	0 to 999

Technical data	
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
S7 timers	128
• Retentive address areas	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
Data areas and their retentive address areas	
Bit memory	128 bytes
• Retentive address areas	Yes
• Preset retentive address areas	MB0 to MB15
Clock memory	8 (1 memory byte)
Data blocks	511 (in the 1 to 511 range of numbers)
• Size	16 Kbytes
Local data per priority class	Max. 256 bytes
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	Max. 16 KB
Nesting depth	
• Per priority class	8
• Additional within an error OB	4
FBs	
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	Max. 16 KB
FCs	
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	Max. 16 KB
Address areas (I/O)	
Total I/O address area	1024 bytes /1024 bytes (can be freely addressed)
I/O process image	128 bytes/128 bytes
Digital channels	Max. 256
Of those central	Max. 256

Technical data	
Analog channels	Max. 64
Of those central	Max. 64
Removal	
Module rack	Max. 1
Modules per rack	Max. 8
Number of DP masters	
• Integrated	None
• Via CP	4
Operable function modules and communication processors	
• FM	Max. 8
• CP (PtP)	Max. 8
• CP (LAN)	Max. 4
Time	
Clock	Yes (SW clock)
• Buffered	No
• Accuracy	Deviation per day < 15 s
• Behavior of the realtime clock after POWER ON	The clock keeps running, continuing at the time-of-day it had when power was switched off.
Operating hours counter	1
• Number	0
• Value range	2^{31} (if SFC 101 is used)
• Granularity	1 hour
• Retentive	Yes; must be manually restarted after every restart
Time synchronization	Yes
• In the PLC	Master
• On MPI	Master/slave
S7 message functions	
Number of stations that can be logged on for signaling functions	6 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	Max. 20
Test and startup functions	
Status/control variables	Yes
• Variables	Inputs, outputs, memory bits, DBs, timers, counters
• Number of variables – Of those as status variable – Of those as control variable	30 30 14

Technical data	
Force	Yes
• Variables	Inputs, outputs
• Number of variables	Max. 10
Block status	Yes
Single-step	Yes
Breakpoints	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	Max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	4
• Number of GD packets – Sender – Receiver	Max. 4 Max. 4 Max. 4
• Size of GD packets – Consistent data	Max. 22 bytes 22 bytes
S7 basic communication	Yes
• User data per job – Consistent data	Max. 76 bytes 76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	
• As server	Yes
• User data per job – Consistent data	Max. 180 bytes (with PUT/GET) 64 bytes
S5compatible communication	Yes (via CP and loadable FCs)
Number of connections	Max. 6
Can be used for	
• PG communication – Reserved (default) – Configurable	Max. 5 1 From 1 to 5
• OP communication – Reserved (default) – Configurable	Max. 5 1 From 1 to 5
• S7-based communication – Reserved (default) – Configurable	Max. 2 2 from 0 to 2
Routing	No
interfaces	
1st interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	No

Technical data	
Interface power supply (15 to 30 VDC)	Max. 200 mA
Functionality	
• MPI	Yes
• PROFIBUS DP	No
• Point-to-point connection	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	No
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication – As server – As client	 Yes No
• Transmission rates	187.5 Kbaud
Programming	
Programming language	LAD/FBD/STL
Instruction set	See the Instruction List
Nesting levels	8
System functions (SFC)	See the Instruction List
System function blocks (SFB)	See the Instruction List
User program protection	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	40 x 125 x 130
Weight	270 g
Voltages, currents	
Power supply (rated value)	DC 24 V
• Permissible range	20.4 V to 28.8 V
Current consumption (no-load operation)	Typically 60 mA
Making current	Typically 2.5 A
Power consumption (nominal value)	0.6 A
I^2t	0.5 A^2s
External fusing of power supply lines (recommended)	Min. 2 A
Power loss	Typically 2.5 W

7.3 CPU 314

Technical data for the CPU 314

Table 7-4 Technical data for the CPU 314

Technical data	
CPU and version	
Order no. [MLFB]	6ES7314-1AF11-0AB0
• Hardware version	01
• Firmware version	V 2.0.0
• Associated programming package	STEP 7 as of V 5.1 + SP 4
Memory	
Work memory	
• Integrated	64 Kbytes
• Expandable	No
Load memory	Plugged in with MMC (Max. 8 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	Guaranteed by MMC (maintenance-free)
Execution times	
Processing times of	
• Bit insructions	Min. 0.1 µs
• Word instructions	Min. 0.2 µs
• Fixed-point arithmetic	Min. 2.0 µs
• Floating-point maths	Min. 3 µs
Timers/counters and their retentive address areas	
S7 counters	256
• Retentive address areas	Configurable
• Default	From C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
S7 timers	256
• Retentive address areas	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)

Technical data	
Data areas and their retentive address areas	
Bit memory	256 bytes
• Retentive address areas	Yes
• Preset retentive address areas	MB0 to MB15
Clock memory	8 (1 memory byte)
Data blocks	
• Number	511 (in the 1 to 511 range of numbers)
• Size	16 Kbytes
Local data per priority class	Max. 510
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	16 Kbytes
Nesting depth	
• Per priority class	8
• Additional within an error OB	4
FBs	See the Instruction List
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	16 Kbytes
FCs	See the Instruction List
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	16 Kbytes
Address areas (I/O)	
Total I/O address area	Max. 1024 bytes/1024 bytes (can be freely addressed)
I/O process image	128 bytes/128 bytes
Digital channels	Max. 1024
Of those central	Max. 1024
Analog channels	Max. 256
Of those central	Max. 256
Removal	
Module rack	Max. 4
Modules per rack	8
Number of DP masters	
• Integrated	None
• via CP	4

Technical data	
Operable function modules and communication processors	
• FM	Max. 8
• CP (PtP)	Max. 8
• CP (LAN)	Max. 10
Time	
Clock	Yes (HW clock)
• Buffered	Yes
• Buffered period	Typically 6 weeks (at an ambient temperature of 104 °F)
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.
• Accuracy	Deviation per day: < 10 s
Operating hours counter	1
• Number	0
• Value range	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	yes; must be manually restarted after every restart
Time synchronization	Yes
• In the PLC	Master
• On MPI	Master/slave
S7 message functions	
Number of stations that can log in for signaling functions (e.g. OS)	12 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	Max. 40
Test and startup functions	
Status/control variables	Yes
• Variables	Inputs, outputs, memory bits, DBs, timers, counters
• Number of variables – Of those as status variable – Of those as control variable	30 30 14
Force	Yes
• Variables	Inputs/Outputs
• Number of variables	Max. 10
Block status	Yes
Single-step	Yes
Breakpoints	2

Technical data	
Diagnostic buffer	Yes
• Number of entries (not configurable)	Max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	4
• Number of GD packets – Sender – Receiver	Max. 4 Max. 4 Max. 4
• Size of GD packets – Consistent data	Max. 22 bytes 22 bytes
S7 basic communication	Yes
• User data per job – Consistent data	Max. 76 bytes 76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	Yes
• As server	Yes
• as client	Yes (via CP and loadable FBs)
• User data per job – Consistent data	Max. 180 (for PUT/GET) 64 bytes
S5compatible communication	Yes (via CP and loadable FCs)
Number of connections	12
Can be used for	
• PG communication – Reserved (default) – Configurable	Max. 11 1 1 to 11
• OP communication – Reserved (default) – Configurable	Max. 11 1 1 to 11
• S7-based communication – Reserved (default) – Configurable	Max. 8 8 0 to 8
Routing	No
interfaces	
1st interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	No
Interface power supply (15 to 30 VDC)	Max. 200 mA

Technical data	
Functionality	
• MPI	Yes
• PROFIBUS DP	No
• Point-to-point connection	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	No
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication – As server – As client	Yes Yes No (but via CP and loadable FBs)
• Transmission rates	187.5 Kbaud
Programming	
Programming language	LAD/FBD/STL
Instruction set	See the Instruction List
Nesting levels	8
System functions (SFC)	See the Instruction List
System function blocks (SFB)	See the Instruction List
User program protection	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	40 x 125 x 130
Weight	280 g
Voltages, currents	
Power supply (rated value)	DC 24 V
• Permissible range	20.4 V to 28.8 V
Current consumption (no-load operation)	Typically 60 mA
Making current	Typically 2.5 A
Power consumption (nominal value)	0.6 A
I^2t	0.5 A^2s
External fusing of power supply lines (recommended)	Min. 2 A
Power loss	Typically 2.5 W

7.4 CPU 315-2 DP

Technical data

Table 7-5 Technical data for the CPU 315-2 DP

Technical data	
CPU and version	
Order no. [MLFB]	6ES7315-2AG10-0AB0
• Hardware version	01
• Firmware version	V 2.0.0
• Associated programming package	STEP 7 as of V 5.1 + SP 4
Memory	
Work memory	
• Integrated	128 Kbytes
• Expandable	No
Load memory	Plugged in with MMC (Max. 8 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	Guaranteed by MMC (maintenance-free)
Execution times	
Processing times of	
• Bit instructions	Min. 0.1 µs
• Word instructions	Min. 0.2 µs
• Integer maths	Min. 2.0 µs
• Floating-point maths	Min. 3 µs
Timers/counters and their retentive address areas	
S7 counters	256
• Retentive address areas	Configurable
• Default	From C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)
S7 timers	256
• Retentive address areas	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB
• Number	unlimited (limited only by RAM size)

Technical data	
Data areas and their retentive address areas	
Bit memory	2048 bytes
• Retentive address areas	Yes
• Preset retentive address areas	MB0 to MB15
Clock memory	8 (1 memory byte)
Data blocks	
• Number	1023 (in the 1 to 1023 range of numbers)
• Size	16 Kbytes
Local data capacity	Max. 1024 bytes per task/510 per block
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	16 Kbytes
Nesting depth	
• Per priority class	8
• Additional within an error OB	4
FBs	See the Instruction List
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	16 Kbytes
FCs	See the Instruction List
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	16 Kbytes
Address areas (I/O)	
Total I/O address area	Max. 2048 bytes / 2048 bytes (can be freely addressed)
Distributed	Max. 2000
I/O process image	128/128
Digital channels	Max. 16384
Of those central	Max. 1024
Analog channels	Max. 1024
Of those central	Max. 256
Removal	
Module rack	Max. 4
Modules per rack	8
Number of DP masters	
• Integrated	1
• Via CP	4

Technical data	
Operable function modules and communication processors	
• FM	Max. 8
• CP (PtP)	Max. 8
• CP (LAN)	Max. 10
Time	
Clock	Yes (HW clock)
• Buffered	Yes
• Buffered period	Typically 6 weeks (at an ambient temperature of 40 °C)
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.
• Accuracy	Deviation per day: < 10 s
Operating hours counter	1
• Number	0
• Value range	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	Yes; must be manually restarted after every restart
Time synchronization	Yes
• In the PLC	Master
• On MPI	Master/slave
S7 message functions	
Number of stations that can log in for signaling functions (e.g. OS)	16 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	40
Test and startup functions	
Status/control variables	Yes
• Variables	Inputs, outputs, memory bits, DBs, timers, counters
• Number of variables – Of those as status variable – Of those as control variable	30 30 14
Force	
• Variables	Inputs/outputs
• Number of variables	Max. 10
Block status	Yes
Single-step	Yes
Breakpoints	2

Technical data	
Diagnostic buffer	Yes
• Number of entries (not configurable)	Max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	8
• Number of GD packets – Sender – Receiver	Max. 8 Max. 8 Max. 8
• Size of GD packets – Consistent data	Max. 22 bytes 22 bytes
S7 basic communication	Yes
• User data per job – Consistent data	Max. 76 bytes 76 bytes (for X_SEND or X_RCV) 64 bytes (for X_PUT or X_GET as the server)
S7 communication	Yes
• As server	Yes
• As client	Yes (via CP and loadable FBs)
• User data per job – Consistent data	Max. 180 bytes (with PUT/GET) 64 byte (as the server)
S5compatible communication	Yes (via CP and loadable FCs)
Number of connections	16
Can be used for	
• PG communication – Reserved (default) – Configurable	Max. 15 1 1 to 15
• OP communication – Reserved (default) – Configurable	Max. 15 1 1 to 15
• S7-based communication – Reserved (default) – Configurable	Max. 12 12 0 to 12
Routing	Yes (Max. 4)
interfaces	
1st interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	No
Interface power supply (15 to 30 VDC)	Max. 200 mA

Technical data	
Functionality	
• MPI	Yes
• PROFIBUS DP	No
• Point-to-point connection	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication – As server – As client	Yes Yes No (but via CP and loadable FBs)
• Transmission rates	187.5 kbps
2nd interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	Yes
Type of interface	Integrated RS485 interface
Interface power supply (15 to 30 VDC)	Max. 200 mA
Functionality	
MPI	No
PROFIBUS DP	Yes
Point-to-point connection	No
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Constant bus cycle time	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission rate	Up to 12 Mbaud
Number of DP slaves per station	124
Address area	Max. 244 bytes

Technical data	
DP slave	
Services	
• PG/OP communication	Yes
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Direct data exchange	Yes
• Transmission rates	Up to 12 Mbaud
• Automatic baud rate search	Yes (only if interface is passive)
• Intermediate memory	244 bytes I / 244 bytes O
• Address areas	Max. 32 with Max. 32 bytes each
• DPV1	No
GSD file	The latest GSD file is available at: http://www.automation.siemens.com/csi/gsd
Programming	
Programming language	LAD/FBD/STL
Instruction set	See the Instruction List
Nesting levels	8
System functions (SFC)	See the Instruction List
System function blocks (SFB)	See the Instruction List
User program protection	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	40 x 125 x 130
Weight	290 g
Voltages, currents	
Power supply (rated value)	DC 24 V
• Permissible range	20.4 V to 28.8 V
Current consumption (no-load operation)	Typically 60 mA
Making current	Typically 2.5 A
Power consumption (nominal value)	0.8 A
I^2t	0.5 A^2s
External fusing of power supply lines (recommended)	Min. 2 A
Power loss	Typically 2.5 W

7.5 CPU 315-2 PN/DP

Technical data

Table 7-6 Technical data for the CPU 315-2 PN/DP

Technical data	
CPU and version	
Order no. [MLFB]	6ES7315-2EG10-0AB0
• Hardware version	01
• Firmware version	V 2.3.0
• Associated programming package	STEP 7 as of V 5.3 + SP 1
Memory	
Work memory	
• Work memory	128 Kbytes
• Expandable	No
Capacity of the retentive memory for retentive data blocks	128 Kbytes
Load memory	Plugged in with MMC (Max. 8 MB)
Buffering	Guaranteed by MMC (maintenance-free)
Data storage life on the MMC (following final programming)	At least 10 years
Execution times	
Processing times of	
• Bit instructions	0.1 µs
• Word instructions	0.2 µs
• Integer maths	2 µs
• Floating-point maths	3 µs
Timers/counters and their retentive address areas	
S7 counters	256
• Retentive address areas	Configurable
• Default	From C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	Unlimited (limited only by work memory)
S7 timers	256
• Retentive address areas	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s

Technical data	
IEC timers	Yes
• Type	SFB
• Number	Unlimited (limited only by work memory)
Data areas and their retentive address areas	
Bit memory	2048 bytes
• Retentive address areas	Configurable
• Preset retentive address areas	From MB0 to MB15
Clock memory	8 (1 memory byte)
Data blocks	
• Number	1023 (in the 1 to 1023 range of numbers)
• Size	16 Kbytes
• Non-Retain support (configured retention)	Yes
Local data per priority class	Max. 1024 bytes per run level / 510 bytes per block
Blocks	
Total	1024 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	16 Kbytes
Nesting depth	
• Per priority class	8
• Additional within an error OB	4
FBs	See the Instruction List
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	16 Kbytes
FCs	See the Instruction List
• Number, Max.	1024 (in the 0 to 2047 range of numbers)
• Size	16 Kbytes
Address areas (I/O)	
Total I/O address area	Max. 2048 bytes / 2048 bytes (can be freely addressed)
Distributed	Max. 2000 bytes
I/O process image	128/128
Digital channels	16384/16384
Of those central	Max. 1024
Analog channels	1024/1024
Of those central	Max. 256

Technical data	
Removal	
Module rack	Max. 4
Modules per rack	8
Number of DP masters	
• Integrated	1
• Via CP	4
Operable function modules and communication processors	
• FM	Max. 8
• CP (PtP)	Max. 8
• CP (LAN)	Max. 10
Time	
Clock	Yes (hardware clock)
• Factory setting	DT#1994-01-01-00:00:00
• Buffered	Yes
• Buffered period	Typically 6 weeks (at an ambient temperature of 40 °C)
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.
• Behavior of the realtime clock after POWER ON	The clock continues running after POWER OFF.
• Accuracy	Deviation per day: < 10 s
Operating hours counter	1
• Number	0
• Value range	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	Yes; must be manually restarted after every restart
Time synchronization	Yes
• In the AS	Master/slave
• On MPI	Master/slave
S7 message functions	
Number of stations that can be logged on for signaling functions	16 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	40

Technical data	
Test and startup functions	
Status/control variables	Yes
• Variables	Inputs, outputs, memory bits, DBs, timers, counters
• Number of variables – Of those as status variable – Of those as control variable	30 Max. 30 Max. 14
Force	
• Variables	Inputs/outputs
• Number of variables	Max. 10
Block status	Yes
Single-step	Yes
Breakpoints	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	Max. 100
Communication functions	
Open IE communication via TCP/IP	Yes (via integrated PROFINET interface and loadable FBs, Max. 8 connections)
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	8
• Number of GD packets – Sender – Receiver	Max. 8 Max. 8 Max. 8
• Size of GD packets – Consistent data	Max. 22 bytes 22 bytes
S7 basic communication	Yes
• User data per job – Consistent data	Max. 76 bytes 76 bytes
S7 communication	Yes
• As server	Yes
• As client	Yes (via integrated PN interface and loadable FBs, or even via CP and loadable FBs)
• User data per job – Consistent data	See the STEP 7 Online Help, *Common parameters of SFBs/FBs and SFC/FC of the S7 communication)*
S5compatible communication	Yes (via CP and loadable FCs)
Number of connections	16
Can be used for	
• PG communication – Reserved (default) – Configurable	Max. 15 1 1 to 15

Technical data	
• OP communication – Reserved (default) – Configurable	Max. 15 1 1 to 15
• S7-based communication – Reserved (default) – Configurable	Max. 14 0 0 to 14
Routing • Interface X1 configured as – MPI – DP master – DP slave (active) • Interface X2 configured as PROFINET	Yes Max. 10 Max. 24 Max. 14 Max. 24
CBA (at 50 % communication load)	
• Maximum data length for arrays and structures between two partners – Acyclic PROFINET interconnections – Cyclic PROFINET interconnections – Local interconnections	 1400 bytes 450 bytes Slave-dependent
• Number of coupled PROFIBUS devices	16
• Total of all master/slave connections	1000
• Number of device-internal and PROFIBUS interconnections	500
• Number of remote interconnecting partners	32
Remote interconnections with acyclical transmission	
Scan rate: Minimum scan interval	500 ms
Number of incoming interconnections	100
Number of outgoing interconnections	100
Remote interconnections with cyclical transmission	
Scan rate: Minimum scan interval	10 ms
Number of incoming interconnections	200
Number of outgoing interconnections	200
HMI interconnections via PROFINET (acyclic)	
HMI interconnections	500 ms
Number of HMI variables	200
Sum of all interconnections	4000 bytes input/4000 bytes output
interfaces	
1st interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	Yes
Interface power supply (15 to 30 VDC)	Max. 200 mA

Technical data	
Functionality	
• MPI	Yes
• PROFIBUS DP	Yes
• Point-to-point connection	No
• PROFINET	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication – As server – As client	Yes Yes No (but via CP and loadable FBs)
• Transmission rates	Max. 12 Mbps
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Constant bus cycle time	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission rate	Up to 12 Mbaud
Number of DP slaves	124
DP slave	
Services	
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Direct data exchange	Yes
• Transmission rates	Up to 12 Mbaud
• Automatic baud rate search	Yes (only if interface is passive)
• Intermediate memory	244 bytes I / 244 bytes O
• Address areas	Max. 32 with Max. 32 bytes each
• DPV1	No

Technical data	
2nd interface	
Type of interface	PROFINET
Physics	Ethernet
electrically isolated	Yes
Autosensing (10/100 Mbps)	Yes
Functionality	
• PROFINET	Yes
• MPI	No
• PROFIBUS DP	No
• Point-to-point connection	No
Services	
• PG communication	Yes
• OP communication	Yes
• S7 communication – Max. configurable interconnections – Maximum number of instances	Yes (with loadable FBs) 14 32
• Routing	Yes
• PROFINET IO	Yes
• PROFINET CBA	Yes
PROFINET IO	
Number of integrated PROFINET IO controllers	1
Number of connectable PROFINET IO devices	128
Max. user data consistency with PROFINET IO	256 bytes
Update Time	1 ms to 512 ms The minimum value is determined by the set communication portion for PROFINET IO, the number of IO devices and the amount of configured user data.
Routing	Yes
S7 protocol functions	
• PG functions	Yes
• OP functions	Yes
• Open IE communication via TCP/IP	Yes
GSD file	The latest GSD file is available at: http://www.automation.siemens.com/csi/gsd
Programming	
Programming language	LAD/FBD/STL
Instruction set	See the Instruction List
Nesting levels	8
System functions (SFC)	See the Instruction List
System function blocks (SFB)	See the Instruction List
User program protection	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	80 x 125 x 130

Technical data	
Weight	460 g
Voltages, currents	
Power supply (rated value)	DC 24 V
• Permissible range	20.4 V to 28.8 V
Current consumption (no-load operation)	100 mA
Making current	Typically 2.5 A
I^2t	Min. 1 A^2s
External fusing of power supply lines (recommended)	Min. 2 A
Power loss	Typically 3.5 W

7.6 CPU 317-2 DP

Technical Data

Table 7-7 Technical data for the CPU 317-2 DP

Technical Data	
CPU and version	
Order number	6ES7317-2AJ10-0AB0
• Hardware version	01
• Firmware version	V 2.1.0
• Associated programming package	STEP 7 as of V 5.2 + SP 1
Memory	
RAM	
• Integrated	512 KB
• Expandable	No
Capacity of the retentive memory for retentive data blocks	Max. 256 KB
Load memory	Plugged in with MMC (Max. 8 MB)
Buffering	Guaranteed by MMC (maintenance-free)
Data storage life on the MMC (following final programming)	At least 10 years
Execution times	
Processing times of	
• Bit operations	0.05 µs
• Word instructions	0.2 µs
• Fixed-point arithmetic	0.2 µs
• Floating-point arithmetic	1.0 µs
Timers/counters and their retentivity	
S7 counters	512

Technical Data	
• Retentive memory	Configurable
• Default	from C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	Unlimited (limited only by work memory)
S7 timers	512
• Retentive memory	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s
IEC Timers	Yes
• Type	SFB
• Number	Unlimited (limited only by work memory)
Data areas and their retentivity	
Flag bits	4096 bytes
• Retentive memory	Configurable
• Default retentivity	From MB0 to MB15
Clock flag bits	8 (1 byte per flag bit)
Data blocks	
• Number	2047 (in the 1 to 2047 range of numbers)
• Size	64 KB
• Non-Retain support (configured retention)	Yes
Local data per priority class	Max. 1024 bytes
Blocks	
Total	2048 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	64 KB
Nesting depth	
• Per priority class	16
• additional within an error OB	4
FBs	See the Instruction List
• Number, Max.	2048 (in the 0 to 2047 range of numbers)
• Size	64 KB

Technical Data	
FCs	See the Instruction List
• Number	2048 (in the 0 to 2047 range of numbers)
• Size	64 KB
Address areas (I/O)	
Total I/O address area	Max. 8192 bytes / 8192 bytes (can be freely addressed)
Distributed	Max. 8192 bytes
I/O process image	256/256
Digital channels	65536/65536
Of those central	Max. 1024
Analog channels	4096/4096
Of those central	256/256
Assembly	
Racks	Max. 4
Modules per rack	8
Number of DP masters	
• Integrated	2
• via CP	4
Number of function modules and communication processors you can operate	
• FM	Maximum 8
• CP (PtP)	Maximum 8
• CP (LAN)	Maximum 10
Time-of-day	
Real-time clock	Yes (HW clock)
• Buffered	Yes
• Buffered period	Typically 6 weeks (at an ambient temperature of 104 °F)
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.
• Accuracy	Deviation per day: < 10 s
Operating hours counter	4
• Number	0 to 3
• Value range	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	yes; must be manually restarted after every restart
Clock synchronization	Yes
• In the PLC	Master/slave
• On MPI	Master/slave

Technical Data	
S7 signaling functions	
Number of stations that can be logged on for signaling functions	32 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	60
Testing and commissioning functions	
Status/control variables	Yes
• Variables	Inputs, outputs, memory bits, DBs, timers, counters
• Number of variables – Of those as status variable – Of those as control variable	30 Maximum 30 Max. 14
Forcing	
• Variables	Inputs/Outputs
• Number of variables	Maximum 10
Block status	Yes
Single step	Yes
Breakpoints	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	Max. 100
Communication functions	
PG/OP communication	Yes
Global data communication	Yes
• Number of GD circuits	8
• Number of GD packets – Sending stations – Receiving stations	Maximum 8 Maximum 8 Maximum 8
• Length of GD packets – Consistent data	Max. 22 bytes 22 bytes
S7 basic communication	Yes
• User data per job – Consistent data	Max. 76 bytes 76 bytes (for X_SEND or X_RCV) 76 bytes (for X_PUT or X_GET as the server)
S7 communication	Yes
• As server	Yes
• as client	Yes (via CP and loadable FBs)
• User data per job – Consistent data	Max. 180 bytes (with PUT/GET) 160 byte (as the server)
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	32

Technical Data	
can be used for	
• PG communication – Reserved (default) – Configurable	Maximum 31 1 1 to 31
• OP communication – Reserved (default) – Configurable	Maximum 31 1 1 to 31
• S7-based communication – Reserved (default) – Configurable	Maximum 30 0 0 to 30
Routing	Yes (Max. 8)
Interfaces	
1st interface	
Type of interface	Integrated RS 485 interface
Physics	RS 485
electrically isolated	Yes
Interface power supply (15 to 30 VDC)	Max. 200 mA
Functionality	
• MPI	Yes
• PROFIBUS DP	Yes
• Point-to-point connection	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication – As server – As client	 Yes No (but via CP and loadable FBs)
• Transmission rates	Max. 12 Mbps
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Constant bus cycle time	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission rates	Up to 12 Mbaud

Technical Data	
Number of DP slaves	124
Address range per DP slave	Max. 244 bytes
DP master (except for DP slave at both interfaces)	
Services	
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Direct data exchange	Yes
• Transmission rates	Up to 12 Mbaud
• Automatic baud rate search	Yes (only if interface is passive)
• Transfer memory	244 bytes I / 244 bytes O
• Address areas	Max. 32 with Max. 32 bytes each
• DPV1	No
2nd interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	Yes
Type of interface	Integrated RS485 interface
Interface power supply (15 to 30 VDC)	Max. 200 mA
Functionality	
MPI	No
PROFIBUS DP	Yes
Point-to-point connection	No
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Constant bus cycle time	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission rates	Up to 12 Mbaud
Number of DP slaves	124
Address area	Max. 244 bytes

Technical Data	
DP master (except for DP slave at both interfaces)	
Services	
• PG/OP communication	Yes
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Direct data exchange	Yes
• Transmission rates	Up to 12 Mbaud
• Automatic baud rate search	Yes (only if interface is passive)
• Transfer memory	244 bytes I / 244 bytes O
• Address areas	Max. 32 with Max. 32 bytes each
• DPV1	No
GSD file	The latest GSD file is available at: http://www.automation.siemens.com/csi/gsd
Programming	
Programming language	LAD/FBD/STL
Available instructions	See the Instruction List
Nesting levels	8
System functions (SFCs)	See the Instruction List
System function blocks (SFBs)	See the Instruction List
User program security	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	80 x 125 x 130
Weight	460 g
Voltages and currents	
Power supply (rated value)	24 VDC
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	Typically 100 mA
Inrush current	Typically 2.5 A
I^2t	1 A^2s
External fusing of power supply lines (recommended)	Min. 2 A
Power loss	Typically 4 W

7.7 CPU 317-2 PN/DP

Technical Data

Table 7-8 Technical data for the CPU 317-2 PN/DP

Technical Data	
CPU and version	
Order number	6ES7317-2EJ10-0AB0
• Hardware version	01
• Firmware version	V 2.3.0
• Associated programming package	STEP 7 as of V 5.3 + SP 1
Memory	
Work memory	
• Work memory	512 KB
• Expandable	No
Capacity of the retentive memory for retentive data blocks	256 KB
Load memory	Plugged in with MMC (Max. 8 MB)
Buffering	Guaranteed by MMC (maintenance-free)
Data storage life on the MMC (following final programming)	At least 10 years
Execution times	
Processing times of	
• Bit operations	0.05 µs
• Word instructions	0.2 µs
• Fixed-point arithmetic	0.2 µs
• Floating-point arithmetic	1.0 µs
Timers/counters and their retentivity	
S7 counters	512
• Retentive memory	Configurable
• Default	from C0 to C7
• Counting range	0 to 999
IEC Counters	Yes
• Type	SFB
• Number	Unlimited (limited only by work memory)
S7 timers	512
• Retentive memory	Configurable
• Default	Not retentive
• Timer range	10 ms to 9990 s

Technical Data	
IEC Timers	Yes
• Type	SFB
• Number	Unlimited (limited only by work memory)
Data areas and their retentivity	
Flag bits	4096 bytes
• Retentive memory	Configurable
• Default retentivity	From MB0 to MB15
Clock flag bits	8 (1 byte per flag bit)
Data blocks	
• Number	2047 (in the 1 to 2047 range of numbers)
• Size	64 KB
• Non-Retain support (configured retention)	Yes
Local data per priority class	Max. 1024 bytes
Blocks	
Total	2048 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
OBs	See the Instruction List
• Size	64 KB
Nesting depth	
• Per priority class	16
• additional within an error OB	4
FBs	See the Instruction List
• Number, Max.	2048 (in the 0 to 2047 range of numbers)
• Size	64 KB
FCs	See the Instruction List
• Number, Max.	2048 (in the 0 to 2047 range of numbers)
• Size	64 KB
Address areas (I/O)	
Total I/O address area	Max. 8192 bytes / 8192 bytes (can be freely addressed)
Distributed	Max. 8192 bytes
I/O process image	
• Configurable	2048/2048
• Default	256/256
Digital channels	65536/65536
Of those central	Max. 1024
Analog channels	4096/4096

Technical Data	
Of those central	256/256
Assembly	
Racks	Max. 4
Modules per rack	8
Number of DP masters	
• Integrated	1
• via CP	4
Number of function modules and communication processors you can operate	
• FM	Maximum 8
• CP (PtP)	Maximum 8
• CP (LAN)	Maximum 10
Time-of-day	
Real-time clock	Yes (hardware clock)
• Factory setting	DT#1994-01-01-00:00:00
• Buffered	Yes
• Buffered period	Typically 6 weeks (at an ambient temperature of 104 °F)
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.
• Behavior of the realtime clock after POWER ON	The clock continues running after POWER OFF.
• Accuracy	Deviation per day: < 10 s
Operating hours counter	4
• Number	0 to 3
• Value range	2^{31} hours (if SFC 101 is used)
• Granularity	1 hour
• Retentive	yes; must be manually restarted after every restart
Clock synchronization	Yes
• In the PLC	Master/slave
• On MPI	Master/slave
S7 signaling functions	
Number of stations that can be logged on for signaling functions	32 (depends on the number of connections configured for PG / OP and S7 basic communication)
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	60

Technical Data	
Testing and commissioning functions	
Status/control variables	Yes
• Variables	Inputs, outputs, memory bits, DBs, timers, counters
• Number of variables – Of those as status variable – Of those as control variable	30 Maximum 30 Maximum 14
Forcing	
• Variables	Inputs/Outputs
• Number of variables	Maximum 10
Block status	Yes
Single step	Yes
Breakpoints	2
Diagnostic buffer	Yes
• Number of entries (not configurable)	Max. 100
Communication functions	
Open IE communication via TCP/IP	Yes (via integrated PROFINET interface and loadable FBs, Max. 8 connections)
PG/OP communication	
Global data communication	Yes
• Number of GD circuits	8
• Number of GD packets – Sending stations – Receiving stations	Maximum 8 Maximum 8 Maximum 8
• Length of GD packets – Consistent data	Max. 22 bytes 22 bytes
S7 basic communication	Yes
• User data per job – Consistent data	Max. 76 bytes 76 bytes
S7 communication	Yes
• As server	Yes
• as client	Yes (via integrated PN interface and loadable FBs, or even via CP and loadable FBs)
• User data per job – Consistent data	See the STEP 7 Online Help, *Common parameters of SFBs/FBs and SFC/FC of the S7 communication)*
S5-compatible communication	Yes (via CP and loadable FCs)
Number of connections	32
can be used for	
• PG communication – Reserved (default) – Configurable	Maximum 31 1 1 to 31

Technical Data	
• OP communication – Reserved (default) – Configurable	Maximum 31 1 1 to 31
• S7-based communication – Reserved (default) – Configurable	Maximum 30 0 0 to 30
Routing • Interface X1 configured as – MPI – DP master – DP slave (active) • Interface X2 configured as – PROFINET	 Yes Maximum 10 Maximum 24 Maximum 14 Maximum 24
CBA (at 50 % communication load)	
• Maximum data length for arrays and structures between two partners – Acyclic PROFINET interconnections – Cyclic PROFINET interconnections – Local interconnections	 1400 bytes 450 bytes Slave-dependent
• Number of coupled PROFIBUS devices	16
• Total of all master/slave connections	1000
• Number of device-internal and PROFIBUS interconnections	500
• Number of remote interconnecting partners	32
Remote interconnections with acyclical transmission	
Scan rate: Minimum scan interval	500 ms
Number of incoming interconnections	100
Number of outgoing interconnections	100
Remote interconnections with cyclical transmission	
Scan rate: Minimum scan interval	10 ms
Number of incoming interconnections	200
Number of outgoing interconnections	200
HMI interconnections via PROFINET (acyclic)	
HMI interconnections	500 ms
Number of HMI variables	200
Sum of all interconnections	4000 bytes input/4000 bytes output
Interfaces	
1st interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	Yes
Interface power supply (15 to 30 VDC)	Max. 200 mA

Technical Data	
Functionality	
• MPI	Yes
• PROFIBUS DP	Yes
• Point-to-point connection	No
• PROFINET	No
MPI	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication – As server – As client	Yes Yes No (but via CP and loadable FBs)
• Transmission rates	Max. 12 Mbps
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Constant bus cycle time	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission speed	Up to 12 Mbps
Number of DP slaves	124
DP master	
Services	
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Direct data exchange	Yes
• Transmission rates	Up to 12 Mbaud
• Automatic baud rate search	Yes (only if interface is passive)
• Intermediate memory	244 bytes I / 244 bytes O
• Address areas	Max. 32 with Max. 32 bytes each
• DPV1	No

Technical Data	
2nd interface	
Type of interface	PROFINET
Physics	Ethernet
electrically isolated	Yes
Autosensing (10/100 Mbps)	Yes
Functionality	
• PROFINET	Yes
• MPI	No
• PROFIBUS DP	No
• Point-to-point connection	No
Services	
• PG communication	Yes
• OP communication	Yes
• S7 communication – Max. configurable connections – Maximum number of instances	Yes (with loadable FBs) 16 32
• Routing	Yes
• PROFINET IO	Yes
• PROFINET CBA	Yes
PROFINET IO	
Number of integrated PROFINET IO controllers	1
Number of connectable PROFINET IO devices	128
Max. user data consistency with PROFINET IO	256 bytes
Update Time	1 ms to 512 ms The minimum value is determined by the set communication portion for PROFINET IO, the number of IO devices and the amount of configured user data.
S7 protocol functions	
• PG functions	Yes
• OP functions	Yes
• Open IE communication via TCP/IP	Yes
GSD file	The latest GSD file is available at: http://www.automation.siemens.com/csi/gsd
Programming	
Programming language	LAD/FBD/STL
Available instructions	See the Instruction List
Nesting levels	8
System functions (SFCs)	See the Instruction List
System function blocks (SFBs)	See the Instruction List
User program security	Yes

Technical Data	
Dimensions	
Mounting dimensions W x H x D (mm)	80 x 125 x 130
Weight	460 g
Voltages and currents	
Power supply (rated value)	24 VDC
• Permitted range	20.4 V to 28.8 V
Current consumption (no-load operation)	100 mA
Inrush current	Typically 2.5 A
I^2t	Min. 1 A^2s
External fusing of power supply lines (recommended)	Min. 2 A
Power loss	Typically 3.5 W

7.8 CPU 319-3 PN/DP

Technical data

Table 7-9 Technical data for the CPU 319-3 PN/DP

Technical data	
CPU and version	
Order no. [MLFB]	6ES7318-3EL00-0AB0
• Hardware version	01
• Firmware version	V 2.4.0
• Associated programming package	STEP 7, V 5.3 + SP3 + HSP or later
Memory/Backup	
work memory	
• Work memory, integrated	1.4 Mbyte
• Work memory, expandable	No
Capacity of the retentive memory for retentive data blocks	700 Kbytes
Load memory	Plugged in with MMC (Max. 8 MB)
Data storage life on the MMC (following final programming)	At least 10 years
Buffering	Up to 700 Kbytes (maintenance-free)
Execution times	
Processing times of	
• Bit instructions, min.	0.01 µs
• Word instructions, min.	0.02 µs
• Fixed-point arithmetic, min.	0.02 µs
• Floating-point arithmetic, min.	0.04 µs

Technical data	
Timers/counters and their retentive address areas	
S7 counters	
• Number	2048
• Retentive address areas, configurable	Yes
• Retentive address areas, preset	From C0 to C7
• Counting range	0 to 999
IEC Counters	
• Available	Yes
• Type	SFB
• Number	Unlimited (limited only by working memory)
S7 timers	
• Number	2048
• Retentive address areas, configurable	Yes
• Retentive address areas, preset	Not retentive
• Timer range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB
• Number	Unlimited (limited only by work memory)
Data areas and their retentive address areas	
Bit memory	
• Number	8192 bytes
• Retentive address areas, configurable	MB 0 to MB 8191
• Preset retentive address areas	MB 0 to MB15
• Number of clock memories	8 (1 memory byte)
Data blocks	
• Number	4095 (in 1 to 4095 range of numbers)
• Size	64 Kbytes
• Non-retain support (configurable retentive address areas)	Yes
Local data per priority class, Max.	1024 bytes
Blocks	
Total number of blocks	4096 (DBs, FCs, FBs) The maximum number of blocks that can be loaded may be reduced if you are using another MMC.
Size, Max.	64 Kbytes

Technical data	
OBs	See the Instruction List
• Size, Max.	64 Kbytes
• Number of free cycle OBs	1 (OB 1)
• Number of time-of-day-interrupt OBs	1 (OB 10)
• Number of delay interrupt OBs	2 (OB 20, 21)
• Number of cyclic interrupt OBs	4 (OB 32, 33, 34, 35)
• Number of process interrupt OBs	1 (OB 40)
• Number of DPV1-interrupt OBs (only DP-CPUs)	3 (OB 55, 56, 57)
• Number of synchrononous cycle interrupt OBs	1 (OB 61)
• Number of asynchronous error interrupts	6 (OB 80, 82, 83, 85, 86, 87) (OB83 only for PN IO)
• Number of startup OBs	1 (OB 100)
• Number of synchronous error interrupt OBs	2 (OB 121, 122)
Nesting depth	
• Per priority class	16
• Additional within an error OB	4
FBs	See the Instruction List
• Number, Max.	2048 (in 0 to 2047 range of numbers)
• Size	64 Kbytes
FCs	See the Instruction List
• Number, Max.	2048 (in 0 to 2047 range of numbers)
• Size	64 Kbytes
Address areas (I/O)	
Total I/O address area	
• Inputs	8 Kbytes
• Outputs	8 Kbytes
• Distributed – Inputs – Outputs	 8 KB 8 KB
Number of sub-process diagrams	1
I/O process image	
• Inputs, configurable	2048 bytes
• Outputs, configurable	2048 bytes
• Inputs, default	256 bytes
• Outputs, default	256 bytes
Digital channels	
• Inputs	65536
• Outputs	65536
• Inputs, central	1024
• Outputs, central	1024

Technical data	
Analog channels	
• Inputs	4096
• Outputs	4096
• Inputs, central	256
• Outputs, central	256
Removal	
Racks, Max.	4
Modules per rack, Max.	8
Number of DP masters	
• Integrated	2
• Via CP	4
Operable function modules and communication processors	
• FM	8
• CP (PtP)	8
• CP (LAN)	10
Time	
Clock	
• Hardware clock	Yes
• Buffered	Yes
• Buffered period	Typically 6 weeks (at an ambient temperature of 104 °F)
• Behavior of the clock on expiration of the buffered period	The clock keeps running, continuing at the time-of-day it had when power was switched off.
• Behavior of the realtime clock after POWER ON	The clock continues running after POWER OFF.
• Accuracy	Deviation per day: < 10 s
Operating hours counter	
• Number	4
• Number	0 to 3
• Value range	0 to 2^{31} hours (using the SFC 101)
• Granularity	1 hour
• Retentive	Yes; must be manually restarted after every restart
Time synchronization	
• supported	Yes
• In the AS	Master/slave
• On MPI	Master/slave
• on Ethernet via NTP	Yes (as client)
S7 message functions	
Number of stations that can be logged on for signaling functions	32 (depends on the number of connections configured for PG / OP and S7 basic communication)

Technical data	
Process diagnostics messages	Yes
• Simultaneously enabled interrupt S blocks	60
Test and startup functions	
Status/control variables	
• Status/control variables	Yes
• Variables	Inputs, outputs, memory bits, DBs, timers, counters
• Maximum number of variables	30
• Number of variables status variables, Max.	30
• Number of variables control variables, Max.	14
Force	
• Force	Yes
• Force, variables	Inputs/outputs
• Force, maximum number of variables	10
Block status	Yes
Single-step	Yes
Number of breakpoints	2
Diagnostic buffer	
• Available	Yes
• Maximum number of entries	100
Communication functions	
Open IE communication	
Number of connections / access points, total	8
TCP/IP	Yes (via integrated PROFINET interface and loadable FBs)
• Maximum number of connections	8
• Data length for connection type 01_H, Max.	1460 bytes
• Data length for connection type 11_H, Max.	8192 bytes
ISO on TCP	Yes (via integrated PROFINET interface and loadable FBs)
• Maximum number of connections	8
• Data length, Max.	8192 bytes
UDP	Yes (via integrated PROFINET interface and loadable FBs)
• Maximum number of connections	8
• Data length, Max.	1472 bytes
PG/OP communication	Yes
Routing	Yes
Global data communication	Yes
• supported	Yes
• Number of GD circuits, Max.	8
• Number of GD packets, Max.	8

Technical data	
• Number of GD packets, sender, Max.	8
• Number of GD packets, receiver, Max.	8
• Size of GD packets, Max.	22 bytes
• Size of GD packets, consistent, Max.	22 bytes
S7 basic communication	
• supported	Yes
• User data per job, Max.	76 bytes
• User data per job, consistent, Max.	64 bytes (for X_SEND or X_RCV), 64 bytes (for X_PUT or X_GET as the server)
S7 communication	
• supported	Yes
• As server	Yes
• As client	Yes (via integrated PN interface and loadable FBs, or even via CP and loadable FBs)
• User data per job – Consistent data	Refer to Step 7 Online Help, *Parameters of SFBs/FBs and SFC/FC of the S7 communication)*
S5compatible communication	
• supported	Yes (via CP and loadable FCs)
Number of connections	
• Total	32
usable for PG communication	31
• PG communication, reserved	1
• PG communication, configurable, Max.	31
usable for OP communication	31
• OP communication, reserved	1
• OP communication, configurable, Max.	31
usable for S7 basic communication	30
• S7 basic communication, reserved	0
• S7 basic communication, configurable, Max.	30
PROFINET CBA	
Reference setting for the CPU communication load	20%
Number of remote interconnecting partners	32
Number of master/slave functions	50
Total of all master/slave connections	3000
Data length of all incoming master/slave connections, Max.	24000 bytes
Data length of all outgoing master/slave connections, Max.	24000 bytes
Number of device-internal and PROFIBUS interconnections	1000
Data length of the device-internal and PROFIBUS interconnections, Max.	8000 bytes

Technical data	
Data length per connection, Max.	1400 bytes
Remote interconnections with acyclical transmission	
• Scan rate: Scan interval, min.	200 ms
• Number of incoming interconnections	100
• Number of outgoing interconnections	100
• Data length of all incoming interconnections, Max.	3200 bytes
• Data length of all outgoing interconnections, Max.	3200 bytes
• Data length per connection, (acyclic interconnections), Max.	1400 bytes
Remote interconnections with cyclic transmission	
• Transmission frequency: Minimium transmission interval	10 ms
• Number of incoming interconnections	300
• Number of outgoing interconnections	300
• Data length of all incoming interconnections, Max.	4800 bytes
• Data length of all outgoing interconnections	4800 bytes
• Data length per connection, (acyclic interconnections), Max.	250 bytes
HMI variables via PROFINET (acyclic)	
• Update HMI variables	500 ms
• Number of stations that can be logged on for HMI variables (PN OPC/iMap)	2xPN OPC / 1x iMap
• Number of HMI variables	600
• Data length of all HMI variables, Max.	9600 bytes
PROFIBUS proxy functionality	
• supported	Yes
• Number of coupled PROFIBUS devices	32
• Data length per connection, Max.	240 bytes (slave dependent)
interfaces	
1st interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	Yes
Interface power supply (15 to 30 VDC)	Max. 150 mA
Functionality	
• MPI	Yes
• DP master	Yes
• DP slave	Yes
• Point-to-point connection	No

Technical data	
MPI	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	Yes
• S7 basic communication	Yes
• S7 communication, as server	Yes
• S7 communication, as client	No (but via CP and loadable FBs)
• Transmission rates	Max. 12 Mbits/s
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Constant bus cycle time support	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission rate	Max. 12 Mbits/s
Number of DP slaves	Max. 124
Address area	
• Inputs, Max.	244 Kbytes
• Outputs, Max.	244 Kbytes
DP slave (except for DP slave at both DP interfaces)	
Services	
• PG/OP communication	Yes
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Direct data exchange	Yes
• DPV1	No
Transmission rates	Up to 12 Mbits/s
Automatic baud rate search	Yes (only if interface is passive)
Intermediate memory	
• Inputs	244 bytes
• Outputs	244 bytes
Address areas	Max. 32
User data per addresss area	Max. 32 bytes

Technical data	
2nd interface	
Type of interface	Integrated RS485 interface
Physics	RS 485
electrically isolated	Yes
Interface power supply (15 to 30 VDC)	Max. 200 mA
Functionality	
MPI	No
DP master	Yes
DP master	Yes
Point-to-point connection	No
DP master	
Services	
• PG/OP communication	Yes
• Routing	Yes
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Constant bus cycle time	Yes
• Isochronous mode	Yes
• SYNC/FREEZE	Yes
• DPV1	Yes
Transmission rate	Up to 12 Mbaud
Number of DP slaves	124
Address area	Max. 244 bytes
DP slave (except for DP slave at both DP interfaces)	
Services	
• PG/OP communication	Yes
• Routing	Yes (only if interface is active)
• Global data communication	No
• S7 basic communication	No
• S7 communication	No
• Direct data exchange	Yes
• DPV1	No
Transmission rates	Up to 12 Mbps
Automatic baud rate search	Yes (only if interface is passive)
Intermediate memory	244 bytes I / 244 bytes O
Address areas	Max. 32 with max. 32 bytes each
GSD file	The latest GSD file is available at: http://www.automation.siemens.com/csi/gsd
3rd. interface	
Type of interface	PROFINET
Physics	Ethernet

Technical data	
electrically isolated	Yes
Autosensing (10/100 Mbaud)	Yes
Functionality	
• PROFINET	Yes
• MPI	No
• PROFIBUS DP	No
• Point-to-point connection	No
Services	
• PG/OP communication	Yes
• S7 communication – Max. configurable interconnections – Maximum number of instances	Yes (with loadable FBs) 16 32
• Routing	Yes
• PROFINET IO	Yes
• PROFINET CBA	Yes
• Open IE communication – via TCP/IP – ISO on TCP – UDP	 Yes Yes Yes
PROFINET IO	
Number of integrated PROFINET IO controllers	1
Number of PROFINET IO devices that can be connected	256
Max. user data consistency with PROFINET IO	256 bytes
Update Rate	1 ms to 512 ms The minimum value is determined by the set communication portion for PROFINET IO, the number of IO devices and the amount of configured user data.
PROFINET CBA	
Acyclic transfer	Yes
Cyclic transfer	Yes
GSD file	The latest GSD file is available at: http://www.automation.siemens.com/csi/gsd
CPU/Programming	
Programming language	STEP 7 as of V5.3
LAD	Yes
FBD	Yes
STL	Yes
SCL	Yes
CFC	Yes
GRAPH	Yes
HiGraph	Yes
Instruction set	See the Instruction List

Technical data	
Nesting levels	8
System functions (SFC)	See the Instruction List
System function blocks (SFB)	See the Instruction List
User program protection	Yes
Dimensions	
Mounting dimensions W x H x D (mm)	120 x 125 x 130
Weight	1250 g
Supply voltage	
Power supply (rated value)	DC 24 V
• Lower limit of admissible range (DC)	20.4 V
• Upper limit of admissible range (DC)	28.8 V
Voltages and currents	
• External fusing of power supply lines (recommended)	Min. 2 A
Current consumption	
• Making current, typically	4 A
• I^2t	1.2 A^2s
• Current consumption (no-load operation), typically	0.4 A
• Power consumption (nominal value), typically	1.05 A
• Power loss, typically	14 W

Appendix

A

A.1 Information about upgrading to a CPU 31xC or CPU 31x

A.1.1 Scope

Who should read this information?

You are already using a CPU from the SIEMENS S7-300 series and now want to upgrade to a new device.

Please note that problems may occur while downloading your user program to the "new" CPU.

If you have used one of the following CPUs in the past ...

CPU	Order number	As of version	
		Firmware	Hardware
CPU 312 IFM	6ES7 312-5AC02-0AB0 6ES7 312-5AC82-0AB0	V1.0.0	01
CPU 313	6ES7 313-1AD03-0AB0	V1.0.0	01
CPU 314	6ES7 314-1AE04-0AB0 6ES7 314-1AE84-0AB0	V1.0.0	01
CPU 314 IFM	6ES7 314-5AE03-0AB0	V1.0.0	01
CPU 314 IFM	6ES7 314-5AE83-0AB0	V1.0.0	01
CPU 315	6ES7 315-1AF03-0AB0	V1.0.0	01
CPU 315-2 DP	6ES7 315-2AF03-0AB0 6ES7 315-2AF83-0AB0	V1.0.0	01
CPU 316-2 DP	6ES7 316-2AG00-0AB0	V1.0.0	01
CPU 318-2 DP	6ES7 318-2AJ00-0AB0	V3.0.0	03

... then please note if you upgrade to one of the following CPUs

CPU	Order number	As of version		Hereafter called
		Firmware	Hardware	
312	6ES7312-1AD10-0AB0	V2.0.0	01	CPU 31xC/31x
312C	6ES7312-5BD01-0AB0	V2.0.0	01	
313C	6ES7313-5BE01-0AB0	V2.0.0	01	
313C-2 PtP	6ES7313-6BE01-0AB0	V2.0.0	01	
313C-2 DP	6ES7313-6CE01-0AB0	V2.0.0	01	
314	6ES7314-1AF10-0AB0	V2.0.0	01	
314C-2 PtP	6ES7314-6BF01-0AB0	V2.0.0	01	
314C-2 DP	6ES7314-6CF01-0AB0	V2.0.0	01	
315-2 DP	6ES7315-2AG10-0AB0	V2.0.0	01	
315-2 PN/DP	6ES7315-2EG10-0AB0	V2.3.0	01	
317-2 DP	6ES7317-2AJ10-0AB0	V2.1.0	01	
317-2 PN/DP	6ES7317-2EJ10-0AB0	V2.3.0	01	
319-3 PN/DP	6ES7318-3EL00-0AB0	V2.4.0	01	

Reference

If you intend to migrate from PROFIBUS DP to PROFINET, we also recommend the following manual: *Programming manual From PROFIBUS DP to PROFINET IO*

See also

DPV1 (Page 3-33)

A.1.2 Changed behavior of certain SFCs

SFC 56, SFC 57 and SFC 13 which work asynchronously

Some of the SFCs that work asynchronously, when used on CPUs 312IFM – 318-2 DP, were always, or under certain conditions, processed after the first call ("quasi-synchronous").

On the 31xC/31x CPUs these SFCs actually run asynchronously. Asynchronous processing may cover multiple OB1 cycles. As a result, a wait loop may turn into an endless loop within an OB.

The following SFCs are affected:

- SFC 56 "WR_DPARM"; SFC 57 "PARM_MOD"

  On CPUs 312 IFM to 318-2 DP, these SFCs always work "quasi-synchronously" during communication with centralized I/O modules and always work synchronously during communication with distributed I/O modules.

Note

If you are using SFC 56 "WR_DPARM" or SFC 57 "PARM_MOD", you should always evaluate the SFC's BUSY bit.

- SFC 13 "DPNRM_DG"

  On CPUs 312 IFM to 318-2 DP, this SFC always works "quasi synchronously" when it is called in OB82. On CPUs 31xC/31x it generally works asynchronously.

Note

In the user program, the job should merely be started in OB 82. The data should be evaluated in the cyclical program, taking account of the BUSY bits and the value returned in RET_VAL.

Hint

If you are using a CPU 31xC/31x, we recommend that you use SFB 54, rather than SFC 13 "DPNRM_DG".

SFC 20 "BLKMOV"

In the past, this SFC could be used with CPUs 312 IFM to 318-2 DP to copy data from a non runtime-related DB.

SFC 20 no longer has this functionality with CPUs 31xC/31x. SFC83 "READ_DBL" is now used instead.

SFC 54 "RD_DPARM"

This SFC is no longer available on CPUs 31xC/31x. Use SFC 102 "RD_DPARA" instead, which works asynchronously.

SFCs that may return other results

You can ignore the following points if you only use logical addressing in your user program.

When using address conversion in your user program (SFC 5 "GADR_LGC", SFC 49 "LGC_GADR"), you must check the assignment of the slot and logical start address for your DP slaves.

- In the past, the diagnostic address of a DP slave was assigned to the slave's virtual slot 2. Since DPV1 was standardized, this diagnostic address has been assigned to virtual slot 0 (station proxy) for CPUs 31xC/31x.
- If the slave has modeled a separate slot for the interface module (e.g. CPU31x-2 DP as an intelligent slave or IM 153), then its address is assigned to slot 2.

Activating / deactivating DP slaves via SFC 12

With CPUs 31xC/31x, slaves that were deactivated via SFC 12 are no longer automatically activated at the RUN to STOP transition. Now they are not activated until they are restarted (STOP to RUN transition).

A.1.3 Interrupt events from distributed I/Os while the CPU status is in STOP

Interrupt events from distributed I/Os while the CPU status is in STOP

With the new DPV1 functionality (IEC 61158/ EN 50170, volume 2, PROFIBUS), the handling of incoming interrupt events from the distributed I/Os while the CPU status is in STOP has also changed.

Previous response by the CPU with STOP status

With CPUs 312IFM – 318-2 DP, initially an interrupt event was noticed while the CPU was in STOP mode. When the CPU status subsequently returned to RUN, the interrupt was then fetched by an appropriate OB (e.g. OB 82).

New response by the CPU

With CPUs 31xC/31x, an interrupt event (process or diagnostic interrupt, new DPV1 interrupts) is acknowledged by the distributed I/O while the CPU is still in STOP status, and is entered in the diagnostic buffer if necessary (diagnostic interrupts only). When the CPU status subsequently returns to RUN, the interrupt is no longer fetched by the OB. Possible slave faults can be read using suitable SSL queries (e.g. read SSL 0x692 via SFC51).

A.1.4 Runtimes that change while the program is running

Runtimes that change while the program is running

If you have created a user program that has been fine-tuned in relation to certain processing times, please note the following points if you are using a CPU 31xC/31x:

- the program will run much faster on the CPU 31xC/31x.
- Functions that require MMC access (e.g. system start-up time, program download in RUN, return of DP station, etc), may sometimes run slower on the CPU 31xC/31x.

A.1.5 Converting the diagnostic addresses of DP slaves

Converting the diagnostic addresses of DP slaves

If you are using a CPU 31xC/31x with DP interface as the master, please note that you may have to reassign the diagnostic addresses for the slaves since the changes to the DPV1 standard sometimes require two diagnostic addresses per slave.

- The virtual slot 0 has its own address (diagnostic address of the station proxy). The module status data for this slot (read SSL 0xD91 with SFC 51 "RDSYSST") contains IDs that relate to the entire slave/station, e.g. the station error ID. Failure and restoration of the station are also signaled in OB86 on the master via the diagnostic address of the virtual slot 0.
- At some of the slaves the interface module is also modeled as a separate virtual slot (for example, CPU as an intelligent slave or IM153), and a suitable separate address is assigned to virtual slot 2.
  The change of operating status is signaled in the master's diagnostic interrupt OB 82 via this address for CPU 31xC-2DP acting as an intelligent slave.

Note

Reading diagnostics data with SFC 13 "DPNRM_DG":
The originally assigned diagnostics address still works. Internally, STEP 7 assigns this address to slot 0.

When using SFC51 "RDSYSST", for example, to read module status information or module rack/station status information, you must also consider the change in slot significance as well as the additional slot 0.

A.1.6 Reusing existing hardware configurations

Reusing existing hardware configurations

If you reuse the configuration of a CPU 312 IFM to 318-2 DP for a CPU 31xC/31x, the CPU 31xC/31x may not run correctly.

If this is the case, you will have to replace the CPU in the STEP 7 hardware configuration editor. When you replace the CPU, STEP 7 will automatically accept all the settings (if appropriate and possible).

A.1.7 Replacing a CPU 31xC/31x

Replacing a CPU 31xC/31x

When supplied, the CPU 31xC/31x adds a connecting plug to the power supply connector.

You no longer need to disconnect the cables of the CPU when you replace a 31xC / 31x CPU. Insert a screwdriver with 3.5 mm blade into the right side of the connector to open the interlock mechanism, then unplug it from the CPU. Once you have replaced the CPU, simply plug the connecting plug back into the power supply connector.

A.1.8 Using consistent data areas in the process image of a DP slave system

Consistent data

The table below illustrates the points to consider with respect to communication in a **DP master system** if you want to transfer I/O areas with "Total length" consistency. You can transfer a maximum of 128 bytes of consistent data.

Table A-1 Consistent data

CPU 315-2 DP (as of firmware 2.0.0), CPU 317, CPU 319 CPU 31xC	**CPU 315-2 DP (as of firmware 1.0.0), CPU 316-2 DP, CPU 318-2 DP (firmware < 3.0)**	**CPU 318-2 DP (firmware >= 3.0)**
The address area of consistent data in the process image is automatically updated.	Even if they exist in the process image, consistent data is not automatically updated.	You can choose whether or not to update the address area of consistent data in the process image.
In order to read and write consistent data you can also use the SFCs 14 and 15 If the address area of consistent data is outside the process image, you have to use the SFCs 14 and 15 to read and write consistent data. Direct access to consistent areas is also possible (e.g. L PEW or T PAW).	To read and write consistent data, you must use SFC14 and 15.	To read and write consistent data, you can also use SFC 14 and SFC 15. If the address area of consistent data is not in the process image, you must use SFC 14 and SFC 15 to read and write consistent data. Direct access to consistent areas is also possible (for example, L PEW or T PAW).

A.1.9 Load memory concept for the CPU 31xC/31x

Load memory concept for the CPU 31xC/31x

On CPUs 312 IFM to 318-2 DP, the load memory is integrated into the CPU and may be extended with a memory card,

The load memory of the CPU 31xC/31x is located on the micro memory card (MMC), and is retentive. When blocks are downloaded to the CPU, they are stored on the MMC and cannot be lost even in the event of a power failure or memory reset.

Reference

See also the *Memory concept* chapter in the *CPU Data 31xC and 31x manual.*

Note

User programs can only be downloaded and thus the CPU can only be used if the MMC is inserted.

A.1.10 PG/OP functions

PG/OP functions

With CPUs 315-2 DP (6ES7315-2AFx3-0AB0), 316-2DP and 318-2 DP, PG/OP functions at the DP interface were only possible if the interface was set to active. With CPUs 31xC/31x, these functions are possible at both active and passive interfaces. The performance of the passive interface is considerably lower, however.

A.1.11 Routing for the CPU 31xC/31x as an intelligent slave

Routing for the CPU 31xC/31x as an intelligent slave

If you use the CPU 31xC/31x as an intelligent slave, the routing function can only be used with an actively-configured DP interface.

In the properties of the DP interface in STEP 7, select the "Test, Commissioning, Routing" check box of the "DP-Slave" option.

A.1.12 Changed retentive behavior for CPUs with firmware >= V2.1.0

Changed retentive behavior for CPUs with firmware >= V2.1.0

For data blocks for these CPUs

- you can set the retentive response in the block properties of the DB.
- Using SFC 82 "CREA_DBL" -> Parameter ATTRIB, NON_RETAIN bit, you can specify if the actual values of a DB should be maintained at POWER OFF/ON or STOP-RUN (retentive DB) or if the start values should be read from the load memory (non-retentive DB).

A.1.13 FMs/CPs with separate MPI address in the central rack of a CPU 315-2 PN/DP, a CPU 317 or a CPU 319-3 PN/DP

FMs/CPs with separate MPI address in the central rack of a CPU 315-2 PN/DP / CPU 317 / CPU 319-3 PN/DP

All CPUs except CPU 315-2 PN/DP, CPU 317, CPU 318-2 DP and CPU 319-3 PN/DP	CPU 315-2 PN/DP, CPU 317 ,CPU 318-2 DP and CPU 319-3 PN/DP
If there are FM/CPs with their own MPI address in the central rack of an S7-300, then they are in the exact same CPU subnet as the CPU MPI station.	If there are FM/CPs with their own MPI address in the central rack of an S7-300, then the CPU forms its own communication bus via the backplane bus with these FM/CPs, which are separated from the other subnets. The MPI address of such an FM/CP is no longer relevant for the stations on other subnets. The communication to the FM/CP is made via the MPI address of the CPU.

When exchanging your existing CPU with a CPU 315-2 PN/DP / CPU 317 / CPU 319-3 PN/DP, you therefore need to

- replace the CPU in your STEP 7 project with the CPU 315-2 PN/DP / CPU 317 / CPU 319-3 PN/DP
- Reconfigure the OPs. The control and the destination address must be reassigned (= the MPI address of the CPU 315-2 PN/DP / CPU 317 CPU 319-3 PN/DP and the slot of the respective FM)
- Reconfigure the project data for FM/CP to be loaded to the CPU.

This is required for the FM/CP in this rack to remain "available" to the OP/PG.

A.1.14 Using loadable blocks for S7 communication for the integrated PROFINET interface

If you have already used S7 communication via CP with loadable FBs (FB 8, FB 9, FB 12 – FB 15 and FC 62 with version V1.0) from the SIMATIC_NET_CP STEP 7 library (these blocks all feature the family type CP300 PBK) and now want to use the integrated PROFINET interface for S7 communication, you must use the corresponding blocks from the Standard Library\Communication Blocks STEP 7 library in your program (the corresponding blocks FB 8, FB 9, FB 12 – FB 15 and FC 62 have at least version V1.1 and family type CPU_300).

Procedure

1. Download and overwrite the old FBs/FCs in your program container with the corresponding blocks from the standard library.
2. Update the corresponding block calls, including updating the instance DBs, in your user program.

Glossary

Application

→ *User program*

Component-Based automation

→ *PROFINET CBA*

CP

→ *Communication processor*

CPU

→ *CPU*

Cyclic interrupt

→ *Interrupt, cyclic interrupt*

Determinism

→ *Real Time*

Device

→ *PROFIBUS Device*

→ *PROFINET Device*

Diagnostics

→ *System diagnostics*

ERTEC

→ *ASIC*

FB

→ *Function block*

FC

→ *Function*

Hub

→ *Switch*

Industrial Ethernet

→ *Fast Ethernet*

Interface, MPI-capable

→ *MPI*

Interrupt, delay

→ *Interrupt, delay*

Interrupt, diagnostic

→ *Diagnostic Interrupt*

Interrupt, process

→ *Process interrupt*

IO controller

→ *PROFINET IO Controller*

→ *PROFINET IO Device*

→ *PROFINET IO Supervisor*

→ *PROFINET IO System*

IO device

→ *PROFINET IO Controller*

→ *PROFINET IO Device*

→ *PROFINET IO Supervisor*

→ *PROFINET IO System*

IO supervisor

→ *PROFINET IO Controller*

→ *PROFINET IO Device*

→ *PROFINET IO Supervisor*

→ *PROFINET IO System*

IO system

→ *PROFINET IO System*

Local data

→ *Data, temporary*

Master

→ *Slave*

MPI address

→ *MPI*

NCM PC

→ *SIMATIC NCM PC*

OB

→ *Organization blocks*

Operating system

→ *CPU*

PC station

→ *SIMATIC PC Station*

PG

→ *Programming device*

PLC

→ *CPU*

PLC

→ *PLC*

PNO

→ *PROFIBUS International*

Process-Related Function

→ *PROFINET Component*

PROFIBUS

→ *PROFIBUS DP*

PROFIBUS

→ *PROFIBUS International*

PROFIBUS Device

→ *Device*

PROFIBUS DP

→ *PROFIBUS*

→ *PROFIBUS International*

PROFINET

Within the framework of Totally Integrated Automation (TIA), PROFINET represents a consequent enhancement of:

- PROFIBUS DP, the established fieldbus and
- Industrial Ethernet, the communication bus for the cell level

Experience gained from both systems was and is being integrated into PROFINET.

PROFINET is an Ethernet-based automation standard of PROFIBUS International (previously PROFIBUS Users Organization e.V.), and defines a multi-vendor communication, automation, and engineering model.

→ *PROFIBUS International*

PROFINET ASIC

→ *ASIC*

PROFINET CBA

Within the framework of PROFINET, PROFINET CBA is an automation concept for the implementation of applications with distributed intelligence.

PROFINET CBA lets you create distributed automation solutions, based on default components and partial solutions.

Component-based Automation allows you to use complete technological modules as standardized components in large systems.

The components are also created in an engineering tool which may differ from vendor to vendor. Components of SIMATIC devices are created, for example, with STEP 7.

PROFINET Device

→ *Device*

PROFINET IO

Within the framework of PROFINET, PROFINET IO is a communication concept for the implementation of modular, distributed applications.

PROFINET IO allows you to create automation solutions, which are familiar to you from PROFIBUS.

That is, you have the same application view in STEP 7, regardless of whether you configure PROFINET or PROFIBUS devices.

PROFINET IO Controller

→ *PROFINET IO Device*

→ *PROFINET IO Supervisor*

→ *PROFINET IO System*

PROFINET IO Device

→ *PROFINET IO Controller*

→ *PROFINET IO Supervisor*

→ *PROFINET IO System*

PROFINET IO Supervisor

→ *PROFINET IO Controller*

→ *PROFINET IO Device*

→ *PROFINET IO System*

PROFINET IO System

→ *PROFINET IO Controller*

→ *PROFINET IO Device*

Proxy

→ *PROFINET Device*

Real Time

→ *Real Time*

Reference ground

→ *Ground*

Repeater

→ *Hub*

Router

→ *Default Router*

→ *Switch*

RT

→ *Real Time*

Segment

→ *Bus segment*

SFB

→ *System function block*

SFC

→ *System function*

Slave

→ *Master*

Substitute

→ *Proxy*

Timer

→ *Timers*

TOD interrupt

→ *Interrupt, time-of-day*

User program

→ *Operating system*

User program

→ *STEP 7*

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SIEMENS

Product Information on

CPU319-3 PN/DP, 6ES7318-3EL00-0AB0

Einleitung

Diese Produktinformation beschreibt Ergänzungen zum Gerätehandbuch CPU31xC und CPU31x, Technische Daten, A5E00105474-06, Ausgabe 01/2006.

Sie finden dieses Handbuch im Internet unter:
http://support.automation.siemens.com/WW/view/de/12996906

Introduction

This product information describes additions to the device manual CPU31xC and CPU31x, Technical Data, A5E00105475-06, issue 01/2006.

You can find this manual on the Internet at:
http://support.automation.siemens.com/WW/view/en/12996906

Introduction

Cette Information Produit décrit les compléments apportés au manuel d'utilisation des CPU31xC et CPU31x, Caractéristiques techniques, A5E00105474-06, édition 01/2006.

Ce manuel se trouve sur Internet à l'adresse :
http://support.automation.siemens.com/WW/view/fr/12996906

Introducción

La presente información de producto describe las ampliaciones realizadas en el manual de producto CPU31xC y CPU31x, Datos técnicos, A5E00105474-06, edición 01/2006.

Encontrará este manual en la siguiente dirección de Internet:
http://support.automation.siemens.com/WW/view/es/12996906

Introduzione

Le presenti informazioni sul prodotto hanno lo scopo di integrare il manuale del prodotto CPU31xC e CPU31x, Dati tecnici, A5E00105474-06, edizione 01/2006.

Il manuale può essere scaricato da Internet all'indirizzo:
http://support.automation.siemens.com/WW/view/it/12996906

A5E00688649-02

Deutsch

Offene Kommunikation über Industrial Ethernet

Die offene Kommunikation über Industrial Ethernet, wird für die CPU 319-3 PN/DP ab der Firmware-Version 2.4.0 um folgende Protokollvarianten erweitert:

- Verbindungsorientiertes Protokoll: ISO on TCP gemäß RFC 1006
- Verbindungsloses Protokoll: UDP gemäß RFC 768

Download der Bausteine für die Protokollvariante UDP gemäß RFC 768

Um mit anderen Kommunikationspartnern per Anwenderprogramm Daten austauschen zu können, stellen wir Ihnen die benötigten Bausteine im Internet zur Verfügung.

Sie finden diese Datei inklusive der Beschreibung im Internet unter:
http://support.automation.siemens.com/WW/view/de/22146612.

Zyklisches Senden auf mehreren OUC-Instanzen

Beim zyklischen Senden auf mehreren OUC-Instanzen mit Sendezyklen < 2,2 ms, kann es zu einer Beeinträchtigung der Kommunikation an der Ethernet-Schnittstelle kommen.

Sollte dies der Fall sein, müssen Sie Ihren Sendezyklus durch untersetzten Aufruf des Sendebausteins verlängern:

- FB63 ”TSEND” für TCP-Senden bzw.
- FB67 ”TUSEND” für UDP-Senden.

Bei weiteren Fragen wenden Sie sich bitte an den Service & Support:
http://support.automation.siemens.com/WW

Einsatz der CPU 319-3 PN/DP mit SINAMICS S120

Beim Einsatz der CPU 319-3 PN/DP mit dem PROFINET-Modul SINAMICS S120 CBE 20 (6SL3055-0AA00-2EB0) benötigen Sie Step 7 V5.4. Erst mit dieser STEP7-Version ist die volle Funktionalität der PROFINET GSDML Version V2 (Multi-API, Physical Device und Multiple Subslots pro Slot) nutzbar.

Word und DWord Zugriffe auf die letzten gültigen Adressen eines Operandenbereichs

Word und DWord Zugriffe auf die letzten gültigen Adressen eines Operandenbereichs verursachen keinen Bereichslängenfehler. Liegt die Anfangsadresse des Zugriffs innerhalb des zulässigen Adressbereichs (E, A, M, L, D), die Endadresse jedoch nicht, so wird in der aktuellen Baugruppenversion kein Bereichslängenfehler (kein Synchronfehler-OB-Aufruf bzw. CPU-Stop) generiert.
Bei Word und DWORD Zugriffen kann somit ein Teil der adressierten Bytes außerhalb des zulässigen Bereichs liegen. Sobald der Zugriff komplett außerhalb des zulässigen Bereichs liegt, wird ein entsprechender Synchronfehler generiert.

Beispiel:

Zugriff auf einen DB mit 100 Byte Länge (DBB0..DBB99)

”T DBD 98” verwendet die Adresse 98...101

Da die Anfangsadresse innerhalb des Operandenbereichs liegt wird kein Bereichslängenfehler erzeugt.
Es erfolgt jedoch auch ein Zugriff auf die nicht vorhandenen Speicheradressen 100 und 101.
Der Inhalt des nicht vorhanden Speicherbereichs ist nach dem Zugriff undefiniert, und darf vom Anwenderprogramm nicht verwendet werden.
Es ist jedoch sichergestellt, dass bei dem Zugriff keine Daten in anderen Operandenbereichen überschrieben werden.

English

Open communication over Industrial Ethernet

The open communication over Industrial Ethernet is upgraded for the CPU 319-3 PN/DP after firmware-version 2.4.0 by the following product variants:

- Connection-oriented log: ISO on TCP according to RFC 1006
- Connectionless log: UDP according to RFC 768

Download of the components for the log variants UDP according to RFC 768

In order to exchange data with other communication partners via application program, we are making the necessary components available to you on the Internet:

You can find these files on the Internet at:
http://support.automation.siemens.com/WW/view/en/22146612

Cyclic transmission to multiple OUC entities

Cyclic transmission to multiple OUC entities with transmission cycles < 2.2 ms can affect communication via the Ethernet interface.

In this case, you must extend your transmission cycle by scaling the calls of the send block:

- FB63 ”TSEND” for TCP transmission or
- FB67 ”TUSEND” for UDP transmission.

For additional information, contact Service & Support via:
http://support.automation.siemens.com/WW

Using CPU 319-3 PN/DP with SINAMICS S120

Use of CPU 319-3 PN/DP in combination with the PROFINET module SINAMICS S120 CBE 20 (6SL3055-0AA00-2EB0) requires STEP 7 V5.4.
This STEP 7 version is required to enable full functionality of the PROFINET GSDML version V2 (multi-API, physical device and multiple subslots per slot).

Word and DWord access to the last valid addresses in an operand range

Word and DWord access to the last valid addresses in an operand range does not result in a length-of-range error. If the initial address lies within the allowable address range (E, A, M, L, D) but the final address lies outside this range, no length-of-range error is generated in the module version (no synchronization error OB call or CPU stop).
For access by Word and DWord, part of the addressed bytes can lie outside the permissible range. Once access is completely outside the permissible range, a corresponding synchronization error is generated.

Example:

Access to a DB with 100 byte length (DBB0 to DBB99)

”T DBD 98” uses the addresses 98 to 101

Since the initial address is within the operand range, no length-of-range error is generated.
However, the non-existent memory addresses 100 and 101 are also accessed. The content of the non-existent memory area is undefined after access, and may not be used by the user program.
This ensures data in other operand ranges is not overwritten during access.

Francais

Communication ouverte via Industrial Ethernet

La communication ouverte via Industrial Ethernet est étendue pour la CPU 319-3 PN/DP à partir du microprogramme-version 2.4.0 aux variantes de protocoles suivantes :

- Protocole orienté liaison : ISO on TCP selon RFC 1006
- Protocole sans liaison : UDP selon RFC 768

Téléchargement des blocs pour la variante de protocole UDP selon RFC 768

Pour permettre l'échange de données avec les autres partenaires de la communication par programme utilisateur, nous vous mettons les blocs nécessaires à disposition sur Internet.

Vous trouverez ce fichier ainsi que la description sur Internet, à l'adresse :

http://support.automation.siemens.com/WW/view/fr/22146612

Emission cyclique sur plusieurs instances OUC

En cas d'émission cyclique sur plusieurs instances OUC avec des cycles d'émission < 2,2 ms, il se peut que la communication à l'interface Ethernet soit entravée.

Si tel est le cas, vous devez augmenter votre cycle d'émission à l'aide d'un appel du bloc d'émission tous les nièmes cycles :

- FB63 "TSEND" pour émission TCP ou
- FB67 "TUSEND" pour émission UDP

Veuillez contacter le Service & Support en cas de question :
http://support.automation.siemens.com/WW

Utilisation de la CPU 319-3 PN/DP avec SINAMICS S120

En cas d'utilisation de la CPU 319-3 PN/DP avec le module PROFINET SINAMICS S120 CBE 20 (6SL3055-0AA00-2EB0), vous avez besoin de STEP7 V5.4.
Ce n'est qu'à partir de cette version de STEP7 que vous pourrez utiliser l'entière fonctionnalité du PROFINET GSDML Version V2 (Multi-API, Physical Device et Multiple Subslots pro Slot).

Accès en Word et DWord à la dernière adresse valable d'une plage d'opérandes

Des accès en Word et DWord à la dernièr adresse valable d'une plage d'opérandes ne provoquent pas d'erreur de longueur de plage. Si l'adresse de début est située au sein de la plage d'adresses autorisée (E, A, M, L, D) mais pas l'adresse de fin, aucune erreur de longueur de plage n'est générée dans la version de module en cours (pas d'appel d'OB d'erreur de synchronisation ou d'arrêt de la CPU).
En cas d'accès en Word et DWORD, une partie des octets adressés peuvent être situés en dehors de la plage autorisée. Dès que l'accès est entièrement situé en dehors de la plage autorisée, une erreur de synchronisation correspondante est générée.

Exemple :

Accès à un DB d'une longueur de 100 octets (DBB0..DBB99)

"T DBD 98" utilise l'adresse 98...101

Comme l'adresse de début est située dans la plage d'opérandes, aucune erreur de longueur de plage n'est générée.
Un accès aux adresses non disponibles 100 et 101 est cependant également effectué.
Le contenu de la plage de mémoire non disponible est indéfini après l'accès et ne doit pas être utilisé par le programme utilisateur.
Il est cependant garanti qu'aucune donnée d'autres plages d'opérandes n'est écrasée lors de l'accès.

Espanol

Comunicación abierta vía Industrial Ethernet

La comunicación abierta vía Industrial Ethernet se amplía para la CPU 319-3 PN/DP con versión de firmware 2.4.0 y superiores con las siguientes variantes de protocolo:

- Protocolo orientado a la conexión: ISO on TCP según RFC 1006
- Protocolo orientado a la no-conexión: UDP según RFC 768

Descarga de bloques para la variante de protocolo UDP según RFC 768

Para poder intercambiar datos con otros interlocutores a través del programa de usuario, ponemos bloques a su disposición en internet.

Encontrará el archivo correspondiente, incluida su descripción en la siguiente dirección de internet:

http://support.automation.siemens.com/WW/view/es/22146612.

Envío cíclico a varias instancias OUC

El envío cíclico a varias instancias OUC en ciclos de envío < 2,2 ms pueden perjudicar la comunicación en la interfaz Ethernet.

En tal caso, es necesario prolongar el ciclo de emisión llamando al bloque de emisión cada ciclo x:

- FB63 ”TSEND” para envío TCP o bien
- FB67 ”TUSEND” para envío UDP.

Para más información, consulte el Service & Support:
http://support.automation.siemens.com/WW

Uso de la CPU 319-3 PN/DP con SINAMICS S120

Para utilizar la CPU 319-3 PN/DP con el módulo PROFINET SINAMICS S120 CBE 20 (6SL3055-0AA00-2EB0) se requiere haber instalado STEP 7 V5.4.
Para aprovechar de una funcionalidad completa de PROFINET GSDML Version V2 (Multi-API, Physical Device und Multiple Subslots pro Slot), debe haberse instalado la presente versión de STEP 7.

Accesos de palabra y de palabra doble a las últimas direcciones válidas de áreas de operando

Accesos de palabra y de palabra doble a las últimas direcciones válidas del área de operandos no provocan ningún error de longitud de área. Si la dirección de inicio del acceso se encuentra comprendida en el área de direccionamiento permitido (E, A, M, L, D), pero la dirección de fin no lo está, no se generará ningún error de longitud de área en la versión de módulo actual (ninguna llamada de OB de errores síncronos o bien STOP de ls CPU).
De este modo, en los accesos de palabra y DWORD, una parte de los bytes direccionados puede encontrarse fuera del área permitida. Tan pronto como el acceso completo se encuentre fuera del área permitida, se genera el error síncrono correspondiente.

Ejemplo:

Acceso a DBs con una longitud de 100 bytes (DBB0..DBB99)

”T DBD 98” utiliza la dirección 98...101

Dado que la dirección de inicio se encuentra comprendida en el área de operandos, no se notifica ningún error de longitud de área.
No obstante tiene lugar el acceso a las direcciones de almacenamiento no disponibles100 y 101.
El contenido del área de almacenamiento no disponible no está definido tras el acceso, y no debe ser utilizado por el usuario.
No obstante se asegura que durante el acceso no se sobrescriban los datos en otras áreas de operandos.

Italiano

Comunicazione aperta tramite Industrial Ethernet

Per la CPU 319-3 PN/DP con versione firmware 2.4.0 o successiva, la comunicazione aperta tramite Industrial Ethernet è stata ampliata con le seguenti varianti di protocollo:

- protocollo orientato al collegamento: ISO on TCP secondo RFC 1006
- protocollo non orientato al collegamento: UDP secondo RFC 768

Download dei blocchi per la variante di protocollo UDP secondo RFC 768

I blocchi che consentono di effettuare lo scambio dei dati con gli altri partner della comunicazione mediante il programma utente sono disponibili in Internet.

I file, completi di descrizione, possono essere scaricati all'indirizzo:

http://support.automation.siemens.com/WW/view/de/22146612.

Trasmissione ciclica di più istanze OUC

Durante una trasmissione ciclica di più istanze OUC con cicli di trasmissione < 2,2 ms può verificarsi un disturbo della comunicazione nell'interfaccia Ethernet.

In questo caso è necessario prolungare il ciclo di trasmissione richiamando un blocco di trasmissione con una frequenza di cicli determinabile:

- FB63 "TSEND" per trasmissione TCP o
- FB67 "TUSEND" per dati UDP.

Per ulteriori informazioni rivolgersi al Service & Support:
http://support.automation.siemens.com/WW

Utilizzo della CPU 319-3 PN/DP con SINAMICS S120

Per utilizzare la CPU 319-3 PN/DP con il modulo PROFINET
SINAMICS S120 CBE 20 (6SL3055-0AA00-2EB0) è necessario disporre della versione V5.4 di Step 7.
Solo con questa versione di STEP7 è possibile usufruire completamente della funzionalità della versione V2 di PROFINET GSDML (Multi-API, Physical Device e Multiple Subslots per ogni Slot).

Accessi Word e DWord agli ultimi indirizzi validi di un’area operando

Gli accessi Word e DWord agli ultimi indirizzi validi di un’area operando non causano alcun errore di lunghezza dell’area. Se l’indirizzo iniziale dell’accesso si trova all’interno dell’area di indirizzo consentita (E, A, M, L, D), ma l’indirizzo finale no, non viene generato alcun errore di lunghezza dell’area nella presente versione dei blocchi (nessun richiamo di OB di errore sincrono o Stop CPU).
In questo modo, con gli accessi Word e DWORD, una parte dei byte indirizzati può trovarsi fuori dell’area consentita. Appena l’accesso si trova completamente fuori dell’area consentita, viene generato un rispettivo errore sincrono.

Esempio:

Accesso ad un DB con lunghezza di 100 Byte (DBB0..DBB99)

”T DBD 98” utilizza l’indirizzo 98...101

Poiché l’indirizzo iniziale si trova all’interno dell’area operando non viene causato alcun errore di lunghezza dell’area.
Tuttavia avviene un accesso anche agli indirizzi di memoria 100 e 101 non presenti.
Il contenuto dell’area di memoria non presente non è difinita dopo l’accesso e non può essere utilizzato dal programma utente.
È comunque sicuro che durante l’accesso non vengano sovrascritti alcuni dati in altre arree operandi.