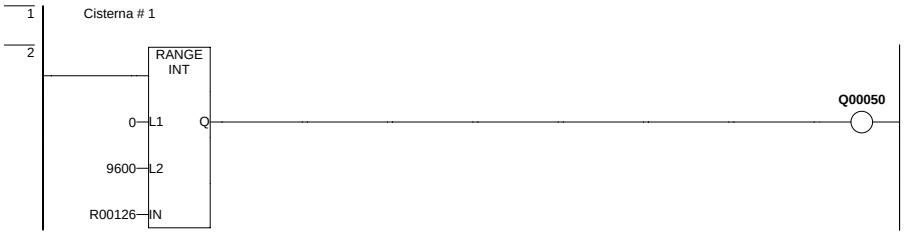


Q00050 %Q00050
LD Block,'cister': NCCON 00011; NOCON 00009, 00011; COIL 00002;
R00126 %R00126
LD Block,'cister': RANGE_INT 00002, 00003, 00004;
LD Block,'N_cist': INT_TO_REAL 00002;

Q00051 %Q00051
LD Block,'cister': COIL 00003;
R00126 %R00126
LD Block,'cister': RANGE_INT 00002, 00003, 00004;
LD Block,'N_cist': INT_TO_REAL 00002;

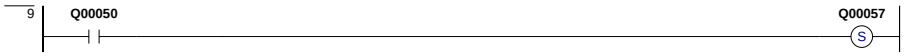
Q00052 %Q00052
LD Block,'cister': NOCON 00010; COIL 00004;
R00126 %R00126
LD Block,'cister': RANGE_INT 00002, 00003, 00004;
LD Block,'N_cist': INT_TO_REAL 00002;

R00132 %R00132
LD Block,'cister': INT_TO_REAL 00005; GT_INT 00008;
R01210 %R01210
LD Block,'cister': MUL_REAL 00006; INT_TO_REAL 00005;

R01212 %R01212
LD Block,'cister': MUL_REAL 00006; REAL_TO_INT 00007;
R01210 %R01210
LD Block,'cister': MUL_REAL 00006; INT_TO_REAL 00005;

R01212 %R01212
LD Block,'cister': MUL_REAL 00006; REAL_TO_INT 00007;
R01214 %R01214
LD Block,'cister': REAL_TO_INT 00007;

Q00056 %Q00056
LD Block,'cister': NOCON 00010; COIL 00008;
R00132 %R00132
LD Block,'cister': INT_TO_REAL 00005; GT_INT 00008;



Q00050 %Q00050
LD Block,'cister': NCCON 00011; NOCON 00009, 00011; COIL 00002;
Q00057 %Q00057
LD Block,'cister': RESETCOIL 00010; SETCOIL 00009;

Q00052 %Q00052
LD Block,'cister': NOCON 00010; COIL 00004;
Q00057 %Q00057
LD Block,'cister': RESETCOIL 00010; SETCOIL 00009;
Q00056 %Q00056
LD Block,'cister': NOCON 00010; COIL 00008;
M00945 %M00945
LD Block,'cister': NOCON 00010; COIL 00011;
M00944 %M00944
LD Block,'cister': NOCON 00010, 00011, 00012;

Q00050 %Q00050
LD Block,'cister': NCCON 00011; NOCON 00009, 00011; COIL 00002;
#T_SEC %S00005
LD Block,'_MAIN': NCCON 00168; NOCON 00047, 00076;
LD Block,'flujo_1': NOCON 00001, 00004;
LD Block,'cister': NOCON 00011, 00023;
LD Block,'genee': NOCON 00015;
R01152 %R01152
LD Block,'cister': UPCTR 00011;
M00945 %M00945
LD Block,'cister': NOCON 00010; COIL 00011;
M00944 %M00944
LD Block,'cister': NOCON 00010, 00011, 00012;

M00944 %M00944
LD Block,'cister': NOCON 00010, 00011, 00012;
Q00436 %Q00436
LD Block,'cister': COIL 00012;

Q00053 %Q00053
LD Block,'cister': NCCON 00023; NOCON 00021, 00023; COIL 00014;
R00129 %R00129
LD Block,'cister': RANGE_INT 00014, 00015, 00016;
LD Block,'N_cist': INT_TO_REAL 00010;

Q00054 %Q00054
LD Block,'cister': COIL 00015;
R00129 %R00129
LD Block,'cister': RANGE_INT 00014, 00015, 00016;
LD Block,'N_cist': INT_TO_REAL 00010;

Q00055 %Q00055
LD Block,'cister': NOCON 00022; COIL 00016;
R00129 %R00129
LD Block,'cister': RANGE_INT 00014, 00015, 00016;
LD Block,'N_cist': INT_TO_REAL 00010;

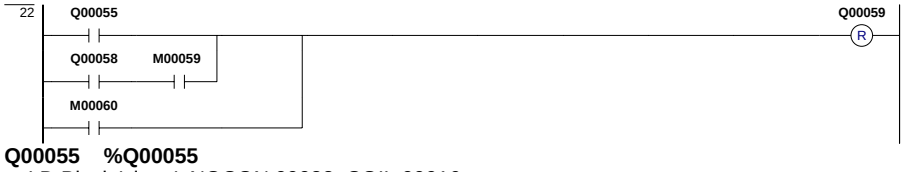
R00135 %R00135
LD Block,'cister': INT_TO_REAL 00017; GT_INT 00020;
R01215 %R01215
LD Block,'cister': MUL_REAL 00018; INT_TO_REAL 00017;

R01217 %R01217
LD Block,'cister': MUL_REAL 00018; REAL_TO_INT 00019;
R01215 %R01215
LD Block,'cister': MUL_REAL 00018; INT_TO_REAL 00017;

R01217 %R01217
LD Block,'cister': MUL_REAL 00018; REAL_TO_INT 00019;
R01219 %R01219
LD Block,'cister': REAL_TO_INT 00019;

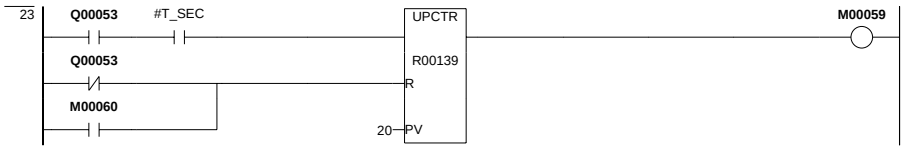
#ALW_ON %S00007
LD Block,'Reloj': NOCON 00001, 00002, 00003, 00004, 00005, 00006, 00007, 00008;
LD Block,'flujo_1': NOCON 00003, 00006;
LD Block,'UMA_N': NOCON 00011, 00102, 00198, 00273, 00395, 00510, 00616;
LD Block,'N_T_ch': NOCON 00001, 00002, 00003, 00004, 00005, 00006, 00007;
LD Block,'N_cist': NOCON 00002, 00003, 00004, 00005, 00006, 00007, 00008, 00010, 00011, 00012, 00013, 00014, 00015, 00016;
LD Block,'cister': NOCON 00020;
LD Block,'genee': NOCON 00011;
LD Block,'incend': NOCON 00026, 00032, 00033, 00034, 00036, 00039, 00040, 00041, 00042, 00043, 00044, 00045;
LD Block,'agua': NOCON 00001, 00002, 00003, 00006, 00007, 00008, 00009, 00010, 00011, 00012, 00020, 00021, 00022, 00031, 00032, 00033;
LD Block,'_MAIN': NOCON 00001, 00002, 00003, 00004, 00005, 00006, 00007, 00008, 00009, 00010, 00011, 00026, 00030, 00033, 00034, 00035, 00049, 00067, 00068, 00078, 00095, 00096, 00121, 00126, 00128, 00129;
Q00058 %Q00058
LD Block,'cister': NOCON 00022; COIL 00020;
R00135 %R00135
LD Block,'cister': INT_TO_REAL 00017; GT_INT 00020;

Q00053 %Q00053
LD Block,'cister': NCCON 00023; NOCON 00021, 00023; COIL 00014;
Q00059 %Q00059
LD Block,'cister': RESETCOIL 00022; SETCOIL 00021;



Q00055 %Q00055
LD Block,'cister': NOCON 00022; COIL 00016;

Q00059 %Q00059
LD Block,'cister': RESETCOIL 00022; SETCOIL 00021;
Q00058 %Q00058
LD Block,'cister': NOCON 00022; COIL 00020;
M00059 %M00059
LD Block,'cister': NOCON 00022; COIL 00023;
M00060 %M00060
LD Block,'cister': NOCON 00022, 00023, 00024;



Q00053 %Q00053
LD Block,'cister': NCCON 00023; NOCON 00021, 00023; COIL 00014;
#T_SEC %S00005
LD Block,'_MAIN': NCCON 00168; NOCON 00047, 00076;
LD Block,'flujo_1': NOCON 00001, 00004;
LD Block,'cister': NOCON 00011, 00023;
LD Block,'genee': NOCON 00015;
R00139 %R00139
LD Block,'cister': UPCTR 00023;
M00059 %M00059
LD Block,'cister': NOCON 00022; COIL 00023;
M00060 %M00060
LD Block,'cister': NOCON 00022, 00023, 00024;

M00060 %M00060
LD Block,'cister': NOCON 00022, 00023, 00024;
Q00437 %Q00437
LD Block,'cister': COIL 00024;